Design Configuration of Circuit and Comparison of Hybrid TFT Op-Amp with its CMOS Counterpart

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Abstract- In this paper, we proposed the design of a Hybrid TFT Operational amplifier using Poly Silicon (Poly Si) TFT, and Amorphous Silicon (a-Si) TFT with MOSFET by using HSPICE Circuit Simulator. The same design also used it with CMOS. The Op-Amps are operating on 3 to 3.3V dc power supply. The designed circuit has been configured with basic concept of op-amp circuit for comparison. The Hybrid OPAMP designed is a two-stage op-amp followed by an output buffer. This Operational Amplifier employs a Miller capacitor and compensated with a current buffer compensation technique. We discussed the design methodology to determine necessary design parameters. In this paper we analyze and compare the results of concepts of op-amp with its circuit configuration.

Keywords— Amorphous Silicon, CMOS, Hybrid, MOSFET, Operational Amplifier, Poly-Silicon, TFT.

I. INTRODUCTION

Thin-film transistors are from Insulated Gate FET family. TFT differs from a typical MOSFET in that it is composed of very thin layer deposited on an insulating substrate, whereas most MOSFETs are formed from a semiconductor wafer. They draws more attention towards the application of different types of TFTs, mainly a-Si, and Poly Si, increases need for an accurately and efficiently to simulate the circuits used on these devices. TFTs are gaining more interest in large area electronics such as flexible displays, RFIDs, sensors, switching systems, solar cells, RAMs, low cost computer logic, flat panel for image crystallization etc,.

By introducing some analytical models, the efforts have been taken to describe the physical characteristics and properties of Organic thin film transistors [1-3]. There were a few efforts reported to have developed an appropriate model describing the OTFTs' characteristics, due to incomplete knowledge of the nature of the carrier transport mechanism in Organic semiconductors [3]. However it is learnt that the electrical characteristics of OTFT are mostly similar to those of a-Si:H TFT. Efforts has been carried out to modify the existing models for a-Si:H TFT in order to represent the characteristics of OTFT [4]. There has been a critical issue with Organic TFT is that they tend to degrade in ambient conditions [5]. Due to low mobility of the TFTs, high performance interface electronics require operational amplifier as the key building block, to be a difficult task. The op-amp has been designed on a-Si:H, which has low gain[6, 7].

This paper is organized into the following sections. The detailed introduction about TFT have been explained in Section I. The Section II, introduces the structures and modelling aspects of thinfilm transistor. In Section III, deals about the Hybrid TFT Operation Amplifier circuit. Design methodology of proposed Hybrid Op-Amps used in various circuit configuration are discussed in section IV. Finally the section V, the result has been concluded for the research work carried out in this paper.

II. STRUCTURE OF TFT

Poly silicon thin film transistors (Poly-Si TFT) have become essential device both in microelectronics and in low cost IC, due to its low temperature process. A leakage current (Ion, off current) present inconsistently in the device, is the problem of poly Si TFT and this current is depend strongly on the bias and temperature which has been generated from grain boundary defects near the drain.an abnormal leakage current is the main deficiency of poly Si TFT. Thus it is very important to research on the leakage current of Poly Si TFT and its reduction. The main reason of the abnormal leakage current is due to the field assisted generation mechanism.

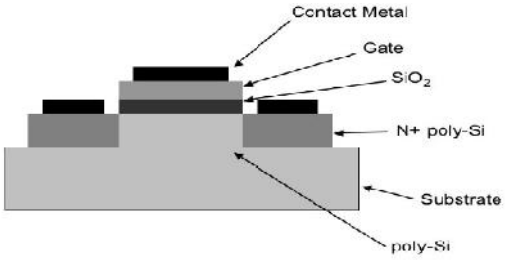


Fig.1. Poly-Si structure with different layers

Fig.1 shows the structure of Poly Si TFT is a kind of three terminal devices; its substrate is floating just like SOI MOSFET. The modeling of Poly Si TFT is the effective medium of approach which treats the non-uniform poly silicon sample with grain boundaries as some uniform effective medium with effective material properties. The increase of drain current in saturation caused by the floating body effect. This short channel devices show a significant decrease of the sub-threshold ideality factor with increasing drain voltage. By using this model, the relations of leakage current between terminal voltages, temperature of the TFT can be obtained.

Fig Fig.2 shows the bottom gate structure of a-Si:H TFT also a three terminal devices. The operation of a-Si TFT is quite different from that of crystalline MOSFETs. In the sub-threshold region the drain current is a poor function of the gate voltage dictated by large trap density in the material while in crystalline MOSFETs. Above threshold most of the induced charge in a-Si:H TFT goes into traps and only a small fraction enters the conduction band. This fraction increases as the gate voltage increases. The field effect mobility increases with the gate voltage.

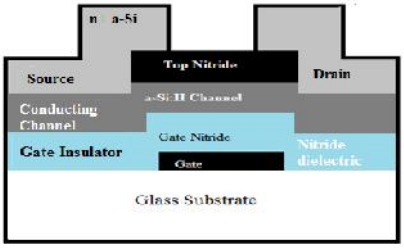


Fig.2. Bottom Gate Structure of an a-Si:H TFT.

The simplest Organic TFT models are very similar to those for conventinal p-channel MOSFETs. The field effect mobility might depend on the channel length and transport properties are very sensitive to the properties of organic semiconductor gate di-electric interface. The structure of the organic p-channel TFTs uses pentacene as the active layer. Aluminum acts as the gate metal and parylene as the gate dielectric [8]. Finally, the devices are encapsulated using a parylene process. The saturation mobility is 0.08 with an on/off current ratio greater than recently, ZnO (and its derivatives) has attracted interest due to its higher mobility and electrical stability [12, 13, 18, 19]. In this paper, we have shown keen interest on Poly Si and a-Si TFTs to use in the Op-Amp, since available literatures organic TFTs are not sufficient.

III. OPERATIONAL AMPLIFIERS

A. Related Work

The CMOS OPAMP is a widely used as analog building block for mixed signal circuits. Many OPAMP design is simple and robust, providing good values for its functional parameters [9, 10]. Palmisano, Palumbo and Pennisi explained about CMOS OPAMP design procedure [14]. This procedure has conditionally allowed using the compensation capacitor for limited range. In this design, Cc is the compensation capacitor greater than a parasitic capacitor Cgs5 of TFT in the OPAMP. The design procedure that allows the Cc a wider range and it would provide a higher degree of freedom in the trade-off between noise and power consumption which have been improved by Mahattanakul and Chutichatuporn [15]. A design procedure of multistage OP-AMP for settling time minimisation with low power is proposed by Pugliese, Cappuccino and Cocorullo [16]. When an OPAMP is necessary to be operated at a high frequency, several limitations have come into the forefront in the existing approaches. The OPAMP designed to work at a low voltage and low power [17]. Although the simulation [19] done in HSPICE shows an operation at a low voltage and it consumes very low power, but the increase observed in the UGF which is not noteworthy to be considered. The multi-stage design [20, 21] leads to the decrease of the phase margin and UGF but it improves the gain and settling time. It is very difficult that the transistors are in saturation condition when the supply voltage decreases[18]. In this research work, an OPAMP has been designed which exhibits high UGF for optimized balancing of gain, speed, power, phase margin, noise and load. Here, the proposed method is to set a higher UGF of the OPAMP working at a lower voltage supply. This permits the value of each circuit element of the amplifier i.e transistor aspect ratios, bias current and compensation capacitor etc,.

B. Operational Amplifiers on TFTs

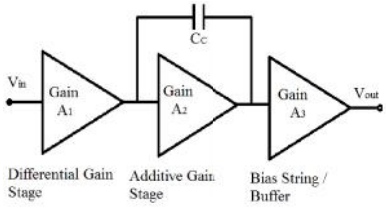


Fig.3. Two Stage CMOS Op-amp

Many operational amplifier systems are incorporating MOSFET transistors in design. This is true in low power and low voltage CMOS Op-Amp analog applications and act as functional core elements of mixed analog and digital nano VLSI circuits and systems. The circuit approach for the implementation of CMOS Op-Amp is the two stage configuration shown in Fig.3. It is designed to provide moderate gain and a relatively low UGF. The differential gain stage includes the input of the Op-amp and provides a overall gain to improve off-set and noise performance.

The additive gain stage is to improve its gain additionally and to allow maximum output swing. The final stage provides proper biasing and act as a buffer to convert high input impedance to low output impedance of additive gain stage and improves the current gain. Capacitor Cc introduced to lower the gain at higher frequencies as a compensating device to achieve stability.

C. Hybrid Op-Amp using TFTs

TFT have higher pinch-off voltage if it compares with almost all the types of FETs. The TFT acts as a switching device in most of the applications. The switching is closed in microseconds and opened it in milliseconds. Like CMOS device characteristics, TFTs are high immunity to noise, operates on low power voltage and low static power consumption. As MOSFET, Significant power is drawn only when TFT device is switching between on and off states and not produce much heat as other forms of logic. These devices also allow a high density of logic functions on a chip.

The proposed hybrid TFT op-amp circuit is shown in Fig.4. The design has been simulated separately as hybrid op-amp using a-Si TFT and Poly Si TFT. TFTs are used as n-type MOSFET and for complementary devices are p-type MOSFET.

In this paper, the proposed design for both the hybrid op-amp using a-Si TFT and Poly-Si TFT improved and implemented to operate in 3 to 3.3V DC power supply and shown its input and output waveforms in common mode configuration in Fig.10 and Fig.16.

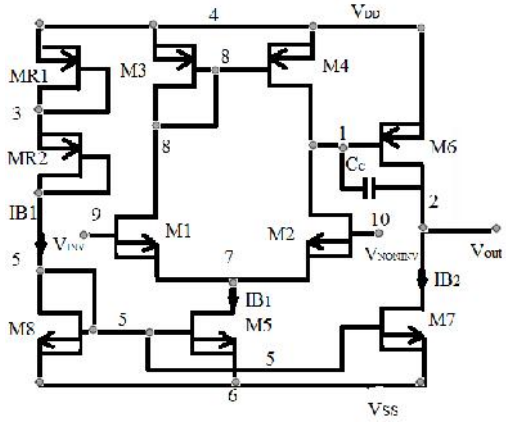


Fig.4. Two stage Hybrid op-amp with n-channel input stage

D. The Design Methodology of Proposed Op-Amp

In the proposed Op-Amp, circuit design is that of a standard CMOS op-amp shown in Fig.4 consists of three stages of circuit- a simple differential pair amplifier for input amplifier, common source amplifier for output amplifier, and a current mirror circuit as a biasing circuit has been chosen for optimising all the parameters.

We adopted a standard common procedure to design the Op-Amp, which are given below:

1. Choose I5 to be as a value which will be decided by slew rate and power dissipation.
2. Find the value of compensation capacitor Cc= I5/Slew Rate.
3. Find gm1 from gain bandwidth =gm1/2π*Cc
4. Find gm5 from condition of stabilitygm5= 2.2*gm1
5. Gain Av={gm1* gam5}/{(gds2+gds4)(gds5+gds7)}
   = {gm1* gam5}/{(λ2+ λ 4)Ids2(λ 5+ λ 7)I7}
6. Calculate I6>(Cc+CL) *SR
7. Find out I6 from step 5 and 6
8. Find (W/L)1,2 from (gm=Sq.Rt{2K(W/L)Ids}
9. Then Find (W/L)5 from (gm=Sq.Rt{2K(W/L)Ids}
10. M3, M4 are matched devices. For matching of the mirror voltages Vds3=Vds4. And since Vgs3=Vds3, and Vds4=Vgs6.
    (W/L)3=(W/L)6*Ids3/Ids6
11. The W/L ratio of current sinks M5 and M7can be found from common current equation of the MOSFET

From the procedure, we determine the following design specification:

1. Determine I_{D5} from the SR specification: $C_c = 1pF$

$$SR = \frac{I_{DS5}}{C_c},\ I_{DS5} = SR * C_c$$

$$V_{DS5(SAT)} = V_{GS5} - |V_{TPO}| = V_{DD} - V_{BIAS} - |V_{TPO}|$$

$$\left(\frac{W}{L}\right)_5 = \frac{2I_{DS5}}{K_P V_{DS5(SAT)}^{\ 2}}$$

$$I_{DS1} = I_{DS2} = \frac{I_{DS5}}{2}$$

2. Determine $(W/L)_1$ from the W_{GB} and positive CMR specification:

$$W_{GB} = \frac{g_{m1}}{C_c} = \frac{1}{C_c}\sqrt{2K_P(W/L)_1 I_{DS1}},$$

$$g_{m1} = C_c * W_{GB}, \qquad \left(\frac{W}{L}\right)_5 = \frac{(g_{m1})^2}{2K_P I_{DS1}}$$

From the positive CMR specification,

$$V_{G1(\max)} = V_{DD} - V_{DS5(SAT)} - V_{GS1}$$

$$V_{GS1} = V_{DD} - V_{DS5(SAT)} - V_{G1(\max)}$$

From the gate bias, V_{bias}, V_{DS5} can be determined.

$$V_{DS1(SAT)} = V_{GS1} - |V_{TPO}|$$

$$\left(\frac{W}{L}\right)_1 = \frac{2I_{DS1}}{K_P V_{DS1(SAT)}^{\ 2}}$$

Select higher (W/L) ratio to satisfy both specifications. We also choose $(W/L)_2 = (W/L)_1$ for matching and symmetry.

3. $(W/L)_3 = (W/L)_4$ from negative CMR

$$\left(\frac{W}{L}\right)_3 = \frac{2I_{DS3}}{K_N (V_{G1(\min)} - V_{SS})^2} = \left(\frac{W}{L}\right)_4$$ Determine

4. Determine $(W/L)_6$ from the PM specification.

$$PM = 90 - \tan^{-1}(W_{GB}/z)\tan^{-1}(W_{GB}/p_2)$$

$$W_{GB} = \frac{g_{m2}}{C_c}; z = \frac{g_{m6}}{C_c}; p_2 = \frac{g_{m6}}{C_1 + C_2}; z > p_2;$$

Since $C_c = C_1 + C_2$

Estimate of PM is obtained by assuming $z = p_2$. That is,

$$PM < 90 - 2\tan^{-1}(\frac{g_{m2}}{C_c}/\frac{g_{m6}}{C_c}) = 90 - 2\tan^{-1}(g_{m2}/g_{m6})$$

$$\tan^{-1}(g_{m2}/g_{m6}) < \frac{90 - PM}{2};$$

$$(g_{m2}/g_{m6}) < \tan\frac{90 - PM}{2};$$

$$g_{m2} < \frac{g_{m6}}{\tan(\frac{90 - PM}{2})};$$

From the equation, $V_{DS1(SAT)} = V_{GS1} - |V_{TPO}|$, we studied to calculate, $V_{DS6(SAT)} = V_{DS3(SAT)}$

$$\left(\frac{W}{L}\right)_6 = \frac{g_{m6}}{K_N V_{DS6(SAT)}^{\ 2}};$$ The current through M_6 is given by $I_{DS6} = \frac{g_{m6}^{\ 2}}{K_N (W/L)_6}$

The current through M_6 must be proper ratio with current through M_3 for balancing, $I_{DS6} = \frac{(W/L)_6}{(W/L)_3} I_{DS3}$.

5. Determine W/L of M_8. First set setup the current source M_8 to 100µA using a biasing current source MR_1 with MR_2.

$$\left(\frac{W}{L}\right)_8 = \frac{I_{DS8}}{K_P (V_{GS8} - |V_{TP}|)^2}$$

E. SIMULATION OF OP-AMP IN HSPICE

The simulation of Op-Amp using the spice parameter specification of MOSFET like a-Si TFT and Poly-Si TFT used in analog and digital circuits. HSPICE model of a-Si TFT and Poly-Si TFT are level 61 and 62 respectively with required parameters given below after calculating their specification.

Spice parameters for

a-Si TFT: NMOS LEVEL=61,

Threshold voltage	=0.9213V,
Saturation modulation parameter	=0.6,
Output conductance parameter	= 0.0008 /V,
Power law mobility parameter	= 0.4 and
Transition width parameter	= 5.0

Poly-Si TFT: NMOS LEVEL=62,

Threshold voltage	=0.6213V,
Proportionality constant of Vsat	=1,
Transition width parameter	=4,
High field mobility	=100 Sq.cm/Vs
Low field mobility parameter	=0.0022 Sq.cm/Vs

IV. CIRCUIT CONFIGURATION

In this paper we discuss about concept of circuit configuration by using Hybrid TFT Op-Amp:

A. Inverting Amplifier Using Hybrid TFT Op- Amp:

Fig.5 shows the design of Inverting amplifier. The positive end of the input voltage V_{in} is connected through a resistor R_1 to the inverting input pin (-) on the op-amp (the negative end of V_{in} is connected to ground) shown in Fig.7. The non-inverting input pin (+) is connected to ground. The gain A_f of the amplifier is defined as the ratio of the output to input voltages.

$$A_f = \frac{V_{out}}{V_{in}}$$

When V_{out} and V_{in} in the above equation represent the actual values of the output and input voltages. When the input is a sinusoidal AC signal, the output will also be a sinusoidal AC signal. For the above circuit, we can assume that the same current flows through both resistors because of the extremely high input impedance and that the voltage at the inverting pin is nearly the same as ground (virtual short). Thus $V_{out} = \frac{R_2}{R_1} V_{in}$ so that the gain will be $A_f = \frac{R_f}{R_1}$. When the input and output are sinusoidal

AC signals, the negative sign in the above equation indicates a 180-degree phase shift between the output and input. Fig.11 and Fig.17 shows its input and output waveforms.

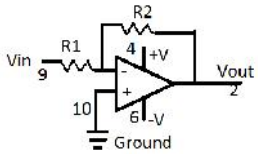


Fig.5. Inverting Amplifier

B. Non Inverting Amplifier Using Hybrid TFT Op- Amp:

Fig.6 shows a simple design for a non-inverting amplifier. The input voltage V_{in} is applied directly to the non-inverting terminal of the op-amp. Negative feedback is provided by the two external resistors R_1 and R_2 which form a voltage divider and apply a fixed fraction of the output voltage to the inverting input terminal of the op-amp. The gain of the amplifier is determined by the external resistors R_1 and R_2 according to the equation:

$$A_f = 1 + \frac{R_2}{R_1}$$

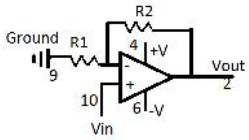


Fig.6. Non Inverting Amplifier

Fig.12 and Fig.18 shows its input and output waveforms.

C. Differential Amplifier Using Hybrid TFT Op- Amp:

In the previous two circuits (inverting and non-inverting amplifiers), there is only one input signal. A differential amplifier is used to deal with two input signals and only the difference between the two input signals is amplified. The circuit shown in Fig.7 is a simple differential amplifier. The two resistors connected to V_1 and V_2 should have the same value (well-matched resistors), and the two resistors, one connected to V_{out} and one connected to ground, should also have the same value. The output signal is related to the two input signals according to the following equation:

$$V_{out} = \frac{R_2}{R_1} V_{in}$$

The gain of the differential amplifier is defined as the ratio between V_{out} and $(V_2 - V)_1$, ie., $A_f = \frac{V_{out}}{V_2 - V_1} = \frac{R_2}{R_1}$. Fig.13 and Fig.19 shows its input and output waveforms.

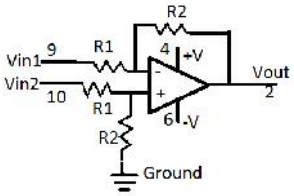


Fig.7. Simple Differential Amplifier

D. Differentiator Using Hybrid TFT Op- Amp:

A differentiator circuit produces an output that is proportional to the derivative or rate of change of the input voltage over time. Differentiator circuit can be constructed as shown in the Fig.8 using an operational amplifier, a resistor, and a capacitor. The output signal is related to the input signals according to the following equation:

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Since the output voltage of a differentiator is proportional to the input frequency, high frequency signals (such as electrical noise) may saturate or cut-off the amplifier. For this reason: a resistor can be placed in series with the capacitor in the input. This establishes high frequency limit beyond which differentiation no longer occurs $f_B = \frac{1}{2\circledR R_{in} C_{in}}$. To achieve greater attenuation at higher frequencies (or prevent oscillation), a feedback capacitor is added in parallel with the feedback resistor. This establishes another break frequency that can be calculated. Fig.14 and Fig.20 shows its input and output waveforms.

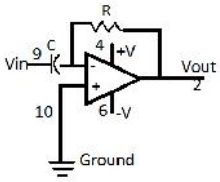


Fig.8: Simple Differentiator

E. Integrator Using Hybrid TFT Op- Amp::

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_f is replaced by a capacitor C_f. The expression for the output voltage is given as, $V_{out} = -(\frac{1}{R_f C_f})\int V_i dt$ Here the negative sign indicates that the output voltage is 180° out of phase with the input signal. Normally between f_a and f_b the circuit acts as an integrator. Generally, the value of $f_a < f_b$. The input signal will be integrated properly if the Time period T of the signal is larger than

or equal to $R_f C_f$. That is $T \geq R_f C_f$. Integrator circuit can be constructed as shown in the Fig.9 using an operational amplifier, a resistor, and a capacitor. Fig.15 and Fig.21 shows its input and output waveforms.

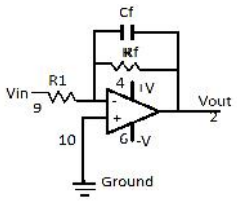


Fig.9: Simple Integrator

V. RESULTS AND DISCUSSION

The proposed model is verified by simulation program with Integrated Circuit Emphasis (HSPICE) is used to simulate and compare with the results predicted by the analytical model.

TABLE 1
W and L values of MOSFET/TFTs

MOSFET/ TFT	W and L values of MOSFET/TFT used in Hybrid OP-AMP using					
	a-Si TFT		Poly-Si TFT		CMOS	
	W (µm)	L (µm)	W (µm)	L (µm)	W (µm)	L (µm)
M1	1000	1	10	1	36	6
M2	1000	1	10	1	36	6
M3	80	1	8	1	5.5	6
M4	80	1	8	1	5.5	6
M5	1000	1	40	1	30	6
M6	600	1	80	1	32	6
M7	1000	1	90	1	90	6
M8	1000	1	40	1	874	6
M9	80	1	8	1	300	6
M10	80	1	8	1	300	6

The two set of results shown in sub division - A indicating the results of Hybrid Poly Si TFT Op-Amp and the sub division –B indicating the results of Hybrid a-Si TFT Op-Amp for the concept of circuit configuration of inverting amplifier, non-inverting amplifier, differential amplifier, differentiator and integrator. Each set of figures shows the input and output waveforms of respective amplifier. Fig.10 and Fig.16 shows the input and output wave forms of respective amplifier on common mode configuration for the verification of their operation at low voltage 3V dc and 3.3V dc power supply.

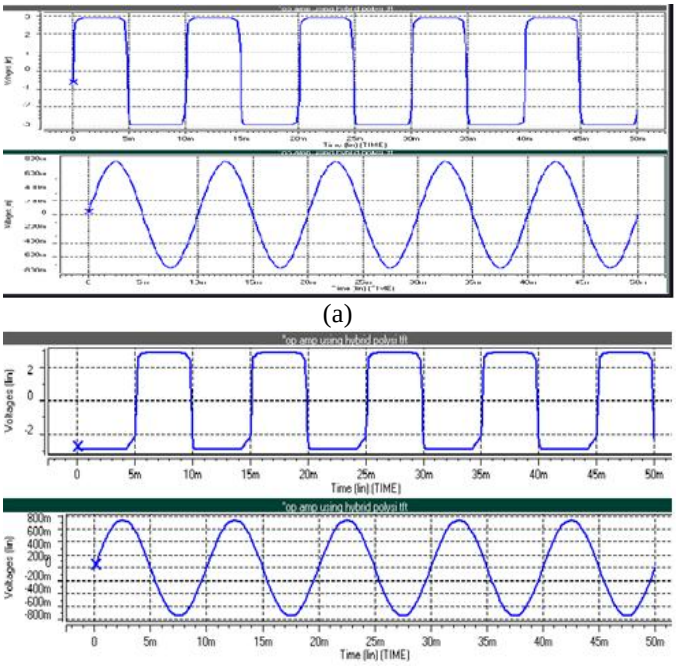
W and L values calculated as per the design procedure explained in this paper for various TFTs and MOSFETs used in the circuit. The result of CMOS Op-Amp are the standard one and their aspect ratio values are shown in table 1 for comparison.Following the required specifications has been used for simulation:

TABLE 2
Specifications, used for simulation

Parameter	Specification		
	a-Si TFT	Poly-Si TFT	CMOS
DD	3.3V DC	3V DC	3V DC
VSS	-3.3V DC	-3V DC	-3V DC
V1	SIN(0V 1VPEAK 4KHZ)		
V2	PWL(0MS 1V 5MS 1V 5.01MS -1V 10MS -1V)		
RF	20K	15K	10K
R1	20K	15K	10K
R2	20K	15K	10K

RESULTS OF HYBRID TFT OP-AMP AFTER SIMULATION IN HSPICE CIRCUIT SIMULATOR

A. Using Poly Si TFT:



(a)

(b)

Fig.10. (a) Input applied in non-inverting input and their corresponding output (b) Input applied in inverting input and their corresponding output

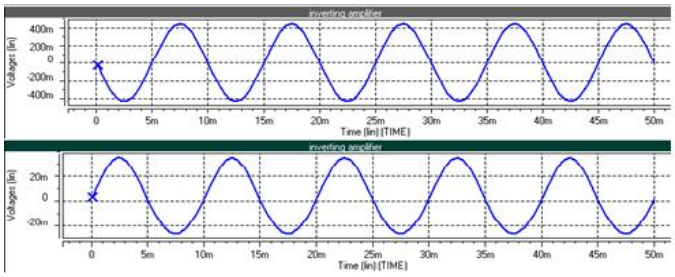


Fig.11: Simulation results of Inverting Amplifier using Hybrid Op-Amp

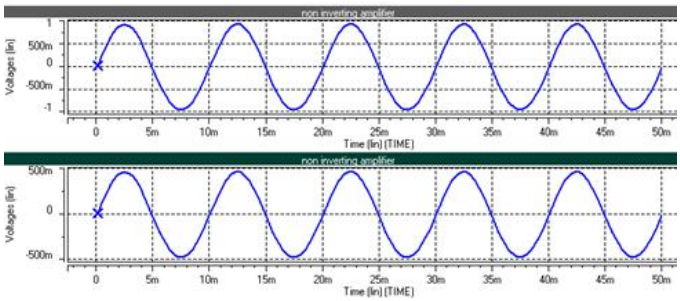


Fig.12: Simulation results of Non Inverting Amplifier using Hybrid Op-Amp

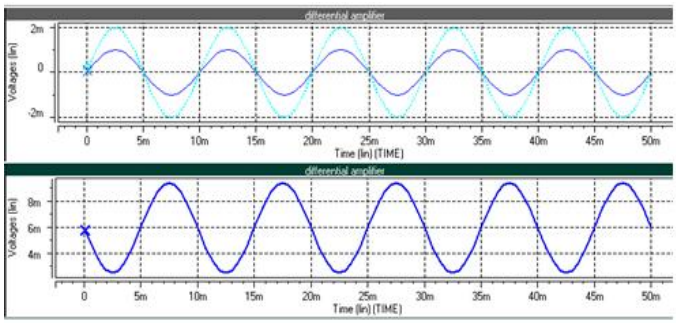


Fig.13: Simulation results of Differential Amplifier using Hybrid Op-Amp

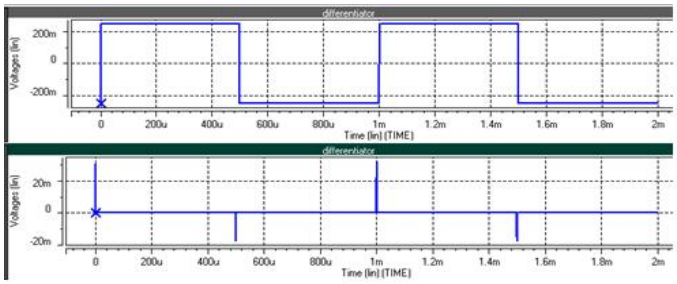


Fig.14: Simulation results of Differentiator using Hybrid Op-Amp

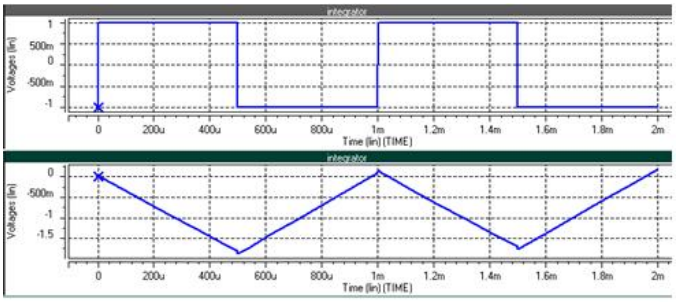
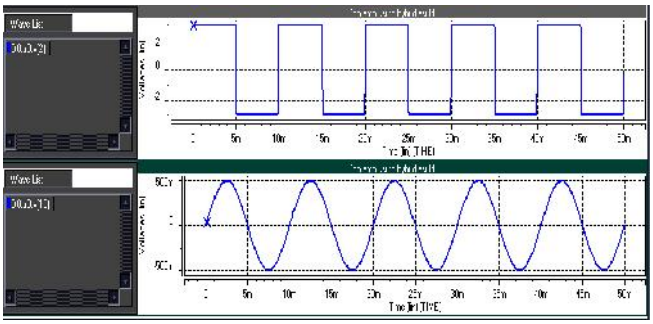
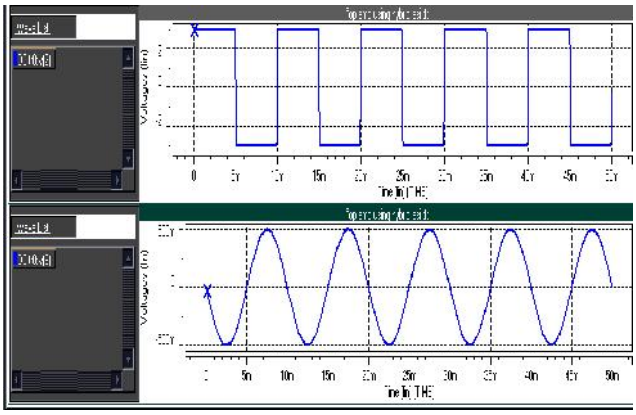


Fig.15: Simulation results of Integrator using Hybrid Op-Amp

B. Using a- Si TFT:



(a)



(b)

Fig.16. (a) Input applied in non-inverting input and their corresponding output (b) Input applied in inverting input and their corresponding output

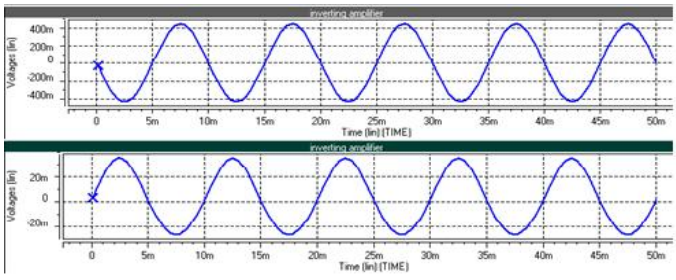


Fig.17: Simulation results of Inverting Amplifier using Hybrid Op-Amp

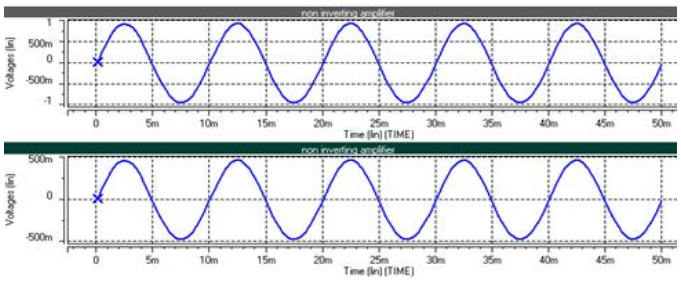


Fig.18: Simulation results of Non Inverting Amplifier using Hybrid Op-Amp

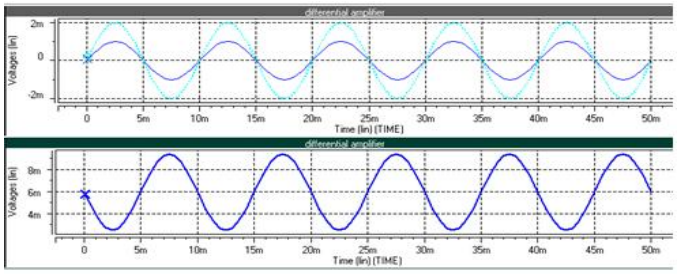


Fig.19: Simulation results of Differential Amplifier using Hybrid Op-Amp

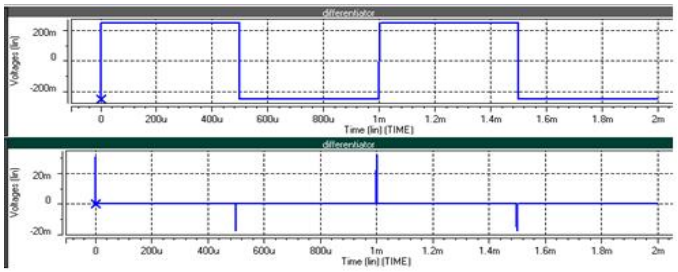


Fig.20: Simulation results of Differentiator using Hybrid Op-Amp

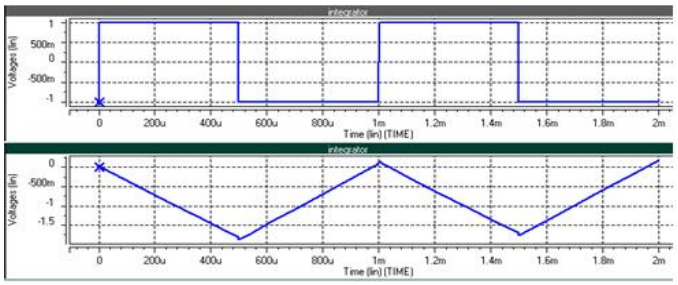


Fig.21: Simulation results of Integrator using Hybrid Op-Amp

Finally, from the Figures 10 to 21, we conclude that the output of various amplifier circuit using Hybrid TFT Op-Amps showing good agreement with CMOS Op-Amps. But the results of output of the circuits using Hybrid Poly-Si TFT Op-Amp is slightly degraded compared with standard CMOS Op-Amp, ie., 0.25V peak to peak lesser. The size of the improvised Hybrid a-Si TFT Op-Amp is 22.92 times bigger than CMOS and Hybrid Poly Si TFT Op-Amps. The Hybrid a-Si TFT is operating with minimum voltage of 3.3V dc power supply and other two Op-Amps are comfortably operating at the minimum voltage of 3V dc power supply

VI. Conclusion

In this paper we have presented the design of Hybrid TFT Op-Amp using Poly-Si TFT, a-Si TFT and CMOS, through the simulation results. The results of inverting amplifier, non-inverting amplifier, differential amplifier, differentiator and integrator of all the three Op-Amps are obtained, evaluated and compared. The results of these amplifiers show an excellent improvement than the CMOS based amplifiers.

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