OPTIMIZATION OF CMOS PARAMETERS BASED ON REVERSIBLE LOGIC GATES

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***Abstract*— Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. This paper provides the basic reversible logic gates, which in designing of more complex system having reversible circuits as a primitive component and which can execute more complicated operations using quantum computers. The reversible circuits form the basic building block of quantum computers as all quantum operations are reversible. This paper presents the data relating to the primitive reversible gates which are available in literature and helps researches in designing higher complex computing circuits using reversible gates.**

***Keywords*— Reversible logic, Reversible gate, Power dissipation, Garbage, Quantum cost,Reversible Computing.**

I. INTRODUCTION

Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systems constructed using irreversible hardware was demonstrated by R. Landauer in the year 1960. According to Landauer's principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmann's constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin[1]. The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods. In 1973, Bennett, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2].

According to Moore's law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information.

The most prominent application of reversible logic lies in quantum computers [3]. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; It has applications in various research areas such as Low Power CMOS design, quantum computing, nanotechnology and DNA computing.

Quantum networks composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, quantum arithmetic must be built from reversible logical components [3]. Reversible computation in a system can be performed only when the system comprises of reversible gates. A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments [4-6].

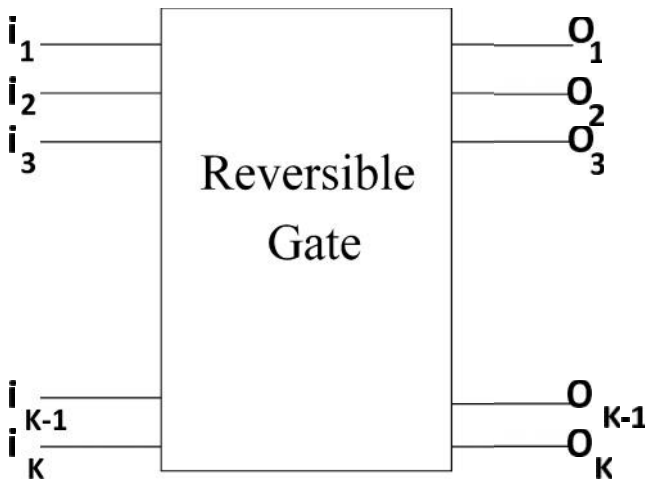


FIG.1 REVERSIBLE LOGIC

An N*N reversible gate can be represented as

Iv=(I1,I2,I3,I4,……IN)

Ov=(O1,O2,O3,……..ON).

Where Iv and Ov represent the input and output vectors respectively. In quantum computing, by considering the need of reversible gates, a literature survey has been done and the mostly available reversible logic gates are presented in this paper.

II. BASIC DEFINITIONS PERTAINING TO REVERSIBLE LOGIC

A.Reversible Function

The multiple output Boolean function *F*(*x*1*; x*2*; :::;xn*) of *n* Boolean variables is called reversible if:

a. The number of outputs is equal to the number of inputs;

b. Any output pattern has a unique pre-image.

B. Reversible logic gate:

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs[8- 10]. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

C. Ancilla inputs/ constant inputs :

This refers to the number of inputs that are to be maintain constant at either 0 or 1 in order to synthesize the given logical function[11].

D. Garbage outputs:

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever necessary. This also refers to the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to achieve reversibility. Garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible. We use the words ―constant inputs‖ to denote the present value inputs that were added to an (n; k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs .

Input + constant input = output + garbage. [7]

E. Quantum cost:

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1 [12].

F. Flexibility :

Flexibility refers to the universality of a reversible logic gate in realizing more functions [13].

G. Gate Level :

This refers to the number of levels in the circuit which are required to realize the given logic functions.

H. Hardware Complexity :

This refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit [14] and [15].

I. Design Constraints for Reversible Logic Circuits:

The following are the important design constraints for reversible logic circuits.

- Reversible logic gates do not allow fan-outs.
- Reversible logic circuits should have minimum quantum cost.
- The design can be optimized so as to produce minimum number of garbage outputs.

- The reversible logic circuits must use minimum number of constant inputs.
- The reversible logic circuits must use a minimum logic depth or gate levels

III. REVERSIBLE LOGIC GATES

There are many number of reversible logic gates that exist at present. The quantum cost of each reversible logic gate is an important optimization parameter [16]. The quantum cost of a 1x1 reversible gate is assumed to be zero while the quantum cost of a 2x2 reversible logic gate is taken as unity. The quantum cost of other reversible gates is calculated by counting the number of V, V+ and CNOT gates present in their circuit. V is the square root of NOT gate and V+ is its Hermitian. The V and V+ quantum gates have the following properties:

V * V = NOT ……. (1)

V * V+ = V+ * V = 1 ……. (2)

V+ * V+ = NOT ……. (3)

Some of the important reversible logic gates are,

1) CNOT GATE

CNOT gate is also known as controlled-not gate. It is a 2*2 reversible gate. The CNOT gate can be described as:

Iv = (A, B) ; Ov = (P= A, Q= A B) Iv and Ov are input and output vectors respectively. Quantum cost of CNOT gate is 1[17]. Figure 2 shows a 2*2 CNOT gate and its symbol.

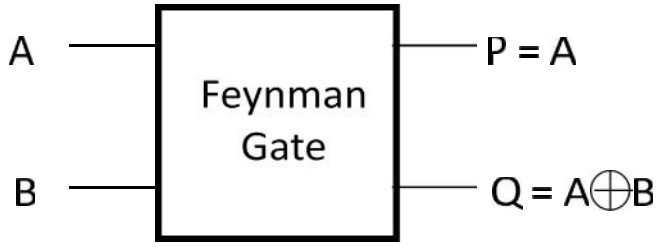


Figure 2: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Table 1: Truth table of Feynman gates

2) Fredkin Gate

Fig 4 shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B AC and R=A′C AB. Quantum cost of a Fredkin gate is 5.

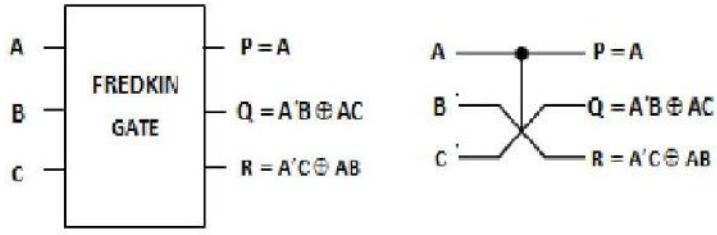


Fig 3: Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

3) Toffoli Gate:

Fig 3 shows a 3*3 Toffoli gate. The input vector is I (A, B, C) and the output vector is O(P,Q,R). The outputs are defined by P=A, Q=B, R=AB C. Quantum cost of a Toffoli gate is 5

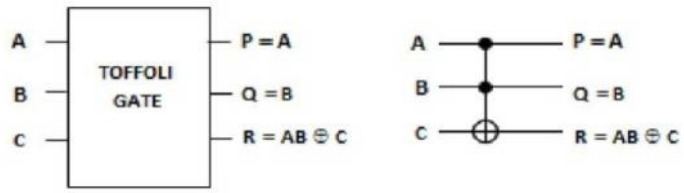


Fig4.Toffoli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Table 3: Truth table of Toffoli gate

IV.Reversible Positive Edge Triggered T Flip-Flop (using Fredkin gate and Feynman Gate)

We proposed the Master-Slave T Flip-Flop using reversible gates such as Fredkin and Feynman. We added a Feynman gate to get the desired functionality of T XOR Q.

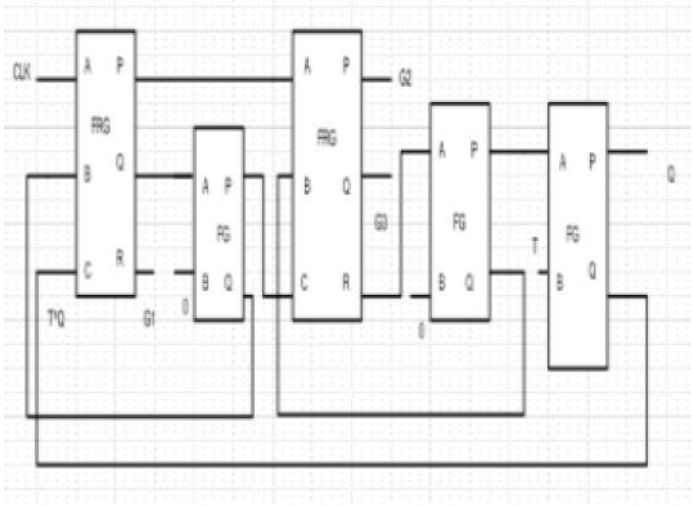
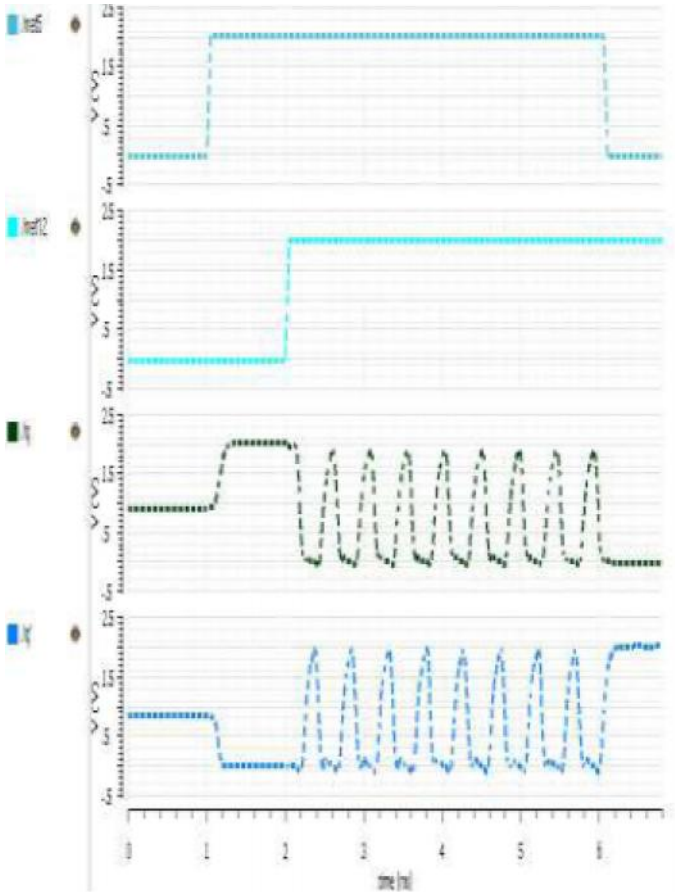


Fig. 5 Reversible positive edge triggered T flip-flop (Fredkin and Feynman gate) In this section we propose the construction of Master-Slave T Flip-Flop using reversible gates. The truth table is shown in the Table 4. The design is shown in the Figure 5. We added a Feynman gate to get the desired functionality of T XOR Q There is no explicit mention of the reversible edge triggered T Flip-Flop. If we do the naive construction by replacing every irreversible gate by appropriate reversible gate, then the number of gates in the design and the garbage outputs will be18.



V.CONCLUSION

The paper proposed the design of a new reversible logic gate which is shown to be advantageous for synthesizing multivalued reversible logic [5]. The paper proposes the designs of the reversible Flip-Flops and Latch using the proposed gate, Fredkin gate and the Feynman gate. The designs are compared with the existing design and are shown to be have an improvement by a factor of 2 to 6. The proposed designs utilized the fact that the reversible circuits constructed from the logic are better in terms of logic complexity and garbage minimization than the one obtained by converting the irreversible designs by replacing gates appropriately. The proposed designs are highly optimized.

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