Stability Estimation of a 5T-SRAM Cell Using Non linear Regression

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***Abstract* _ SRAM Plays a major role for memory based applications in the range of large static noise margin. The noise present at the SRAM causes read and writes operation delays. we are going to estimate the noise margin level and the stability of the 6T SRAM while on the read and write mode of operation. The data given to the circuit causes more stability and reliability for the high Static noise margin. The leakage of this circuit from the N-MOS or P-MOS causes the low reliability, stability and also causes more power consumption. The 6T-SRAM with virtual ground is used to reduce the leakage from the transistor at the read and write operation. The circuit is to designed at 45 nm CMOS process and analyzed in TANNER T-SPICE Simulations. The leakage of this circuit from the N-MOS or P-MOS causes the low reliability, stability and also causes more power consumption. The 6T-SRAM with virtual ground is used to reduce the leakage from the transistor at the read and write operation. The circuit can be analyzed in TANNER T-SPICE Simulations**

Keywords: 5T,6T,Static noise margin, Read ability, write stability.

I. INTROD UCTION

SRAM cell design has to cope with a stringent constraint on the cell area to achieve high integration density in modern system-on-chips (SoCs). This leads to choosing min- imal width-to-length ratios for the SRAM cell transistors. As dimensions scale down to nanometer regime, the variations in CMOS transistor parameters, e.g., the threshold voltage ,

increase steadily due to random dopant density fluctuations in channel, source and drain. Therefore, two closely placed, supposedly identical transistors, have important differences in their electrical parameters as and make the design of the SRAM less predictable and controllable. Moreover, the stability of the SRAM cell is seriously affected by the increase in variability and by the decrease in supply voltage . In the past there has been considerable effort in understanding and modeling the stability of the SRAM cell. Several analytical models of the static noise margin (SNM) have been developed to optimize the cell design, to predict the effect of parameter changes on the SNM and to assess the impact of intrinsic parameter variations on the cell stability . Furthermore, new SRAM cell circuit designs have been developed to maximize.

The standard setup for the SNM definition is shown. The two DC noise voltage sources V are placed in series with the cross-coupled inverters and with worst-case polarity at the internal nodes V and V of the SRAM cell.The cell stability for future technology nodes. Little work has been published on an alternative definition of cell stability based on the SRAM cell N-curve . In this paper, we analyze and model this N-curve definition and we compare it with the SNM. We demonstrate that the N-curve contains information both on the read stability and on the write-ability, thus allowing a complete functional analysis of the SRAM cell with only one N-curve (Section II). To our knowledge, this extension in using the N-curve for the write-ability is reported here for the first time. Analytical models of the N-curve metrics for the read stability and write-ability of the cell are derived in Section III by using a classical deep-submicron (DSM) transistor model. We also describe in this section the possible tradeoffs between the different N-curve metrics. Finally, these N-curve metrics are used in Section IV to investigate the impact of variability on the cell; we derive new design criteria for the SRAM cell affected by intra-die variations, based on a statistically-aware optimization approach.

READ STABILITY AND WRITE-ABILITY OF THE SRAM CELL

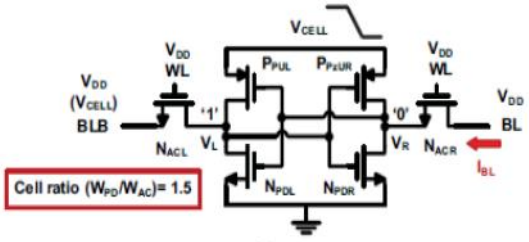
The SRAM Cell Read Stability

Data retention of the SRAM cell, both in standby mode and during a read access, is an important functional constraint in advanced technology nodes. The cell becomes less stable with lower supply voltage, increasing leakage currents and in- creasing variability, all resulting from technology scaling. The stability is usually defined by the SNM as the maximum value of DC noise voltage that can be tolerated by the SRAM cell without changing the stored

bit. In the equivalent circuit for the SNM definition is shown. The two DC noise voltage sources are placed in series with the cross-coupled inverters and with worst-casepolarityattheinternalnodes of the cell. Locating the smallest square between the two largest ones delimited by the eyes of the butterfly curve determines graphi-cally the SNM When is equal to the SNM, the VTCs move horizontally and/or vertically until the stable point A.

II. *Existing System*

Read and write noise Margin for the conventional SRAM is low. Read and write stability of the circuit is low when data=1.The BITLINE leakage is high for N-MOS and P-MOS Transistor. Due to the BITLINE leakage the power consumption is high. Read Retension Voltage(RRV) is measured by changing the cell supply or word-line driver supply. The amount of the supply voltage scaling is recorded as Static Read Retention Voltage(SRRV). In 6T SRAM cell power consumption and leakage is more. so we have to design Minimum number of transistor based SRAM cell design rules without any performance degradation. Here we have to design 5T SRAM design improvement in performance of the proposed cell as regards performance parameters like delay, power consumption and leakage current**.**

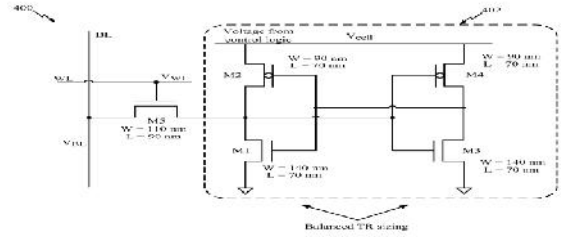


Proposed system

- 5T SRAM deign based on idle mode operation

Data is read and written from BL (Bit line) through transmission gate whose controlling signals are WL and WLB (Word lines). During idle mode of cell transmission gate is OFF. When '1' is stored in cell, Transistor NM1 is ON and STB node pulled down to GND. Bit '1' is stored at ST node uses leakage current from BL through transmission gate and storage of charge at the node due to various capacitances of MOS transistor and wires.

A 5 Transistor Static Random Access Memory is designed for reduced cell size and immunity to process variation. The 5T SRAM includes a storage element for storing data, where in the storage element is coupled to a first voltage and a ground voltage. The storage element can include symmetrically sized cross-coupled inverters. A single access transistor controls read and write operations on the storage element. Control logic is configured to generate a value of the first voltage a write operation that is different from the value of the first voltage for a read operation. SRAM cells are fast and do not need to be dynamically updated, as in the case of Dynamic Random Access Memory (DRAM) cells. The structure of a conventional SRAM cell comprises two cross-coupled inverters, conventionally formed from four Complementary Metal Oxide Semiconductor (CMOS) transistors.



OPERATION IN 5T-SRAM

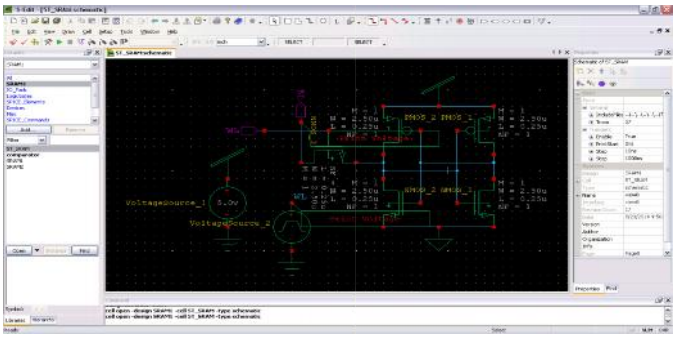
Before the onset of a read operation, the word line is held low and the bitline is precharged.The bitline is not precharged to VCC, So another value is carefully chosen according to stability and performance requirements.

Read Operation-The operation scheme when reading a 5T cell is very similar to the 6T SRAM.If reading a '0', BL will now be pulled down through the transistor combination. If instead a '1' is to be read, the situation is slightly different from the 6T case

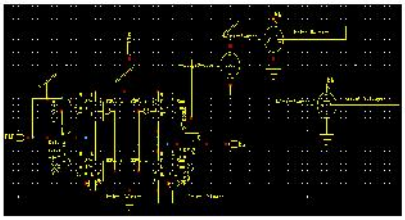
Write Operation-

Writing in the 5T SRAM cell differs from the 6T cell mainly by the fact that it is done from only one bitline.In the 5T cell the value to be written is held on the bitline, and the word line is asserted. The 6T cell was sized so that a '1' could not be written by a high voltage on the bitline, the 5T cell has to be sized differently.

Result analysis



5T SRAM CELL



6T SRAM

Comparison

In 6T SRAM cell power consumption is more .So we have to design Minimum number of transistor based SRAM cell design rules without any performance degradation. Here we have to design 5T SRAM design improvement in performance of the proposed cell as regards performance parameters like delay, power consumption and leakage current.

Conclusion

The stability estimation of a 6T-SRAM cell using a nonlinear regression from cell currents under variant supply levels. This technique can be applied in real IC, the modified measurable failure conditions. This technique can be implemented in a modern CMOS SRAM chip with small extra cost for the area of the measurement circuitry without the change of the SRAM array structure.

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REFERENCE

[1] J. Hicks, D. Bergstrom, M. Hattendorf, J. Jopling, J. Maiz, S. Pae, C. Prasad, and J. Wiedemer"45 nm transistor reliability," Int. Technol. J., vol. 12, no. 2, pp. 131–144, Jun. 2008.

[2] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," IEEE J. Solid-State Circuits, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[3] A. J. Bhavnagarwala, X. Tang, and J. D. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," IEEE J. Solid-State Circuits, vol. 36, no. 4, pp. 658–665, Apr. 2001.

[4] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," IEEE J. Solid-State Circuits, vol. 22, no. 5, pp. 748–754, Oct. 1987.

[5] A. J. Bhavnagarwala, S. Kosonocky, C. Radens, C. Yuen, K. Stawiasz, U. Srinivasan, S. P. Kowalczyk, and M. M. Ziegler, "A sub-600-mV, fluctuation tolerant 65-nm CMOS SRAM array with dynamic cell Biasing," IEEE J. Solid-State Circuits, vol. 43, no. 4, pp. 946–955, Apr. 2008.

[6] J. Wang, S. Yaldiz, X. Li, and L. T. Pileggi, "SRAM parametric failure analysis," in Proc. ACM/IEEE 46th Design Automat. Conf., 2009, pp. 496–501.

[7] R. Kanj, R. Joshi, and S. Nassif, "Mixture importance sampling and its application to the analysis of SRAM designs in the presence of rare failure events," in Proc. ACM/IEEE 43rd Design Automat. Conf., 2006, pp. 69–72.

[8] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read stability and write-ability analysis of SRAM cells for nanometer technologies," IEEE J. Solid-State Circuits, vol. 41, no. 11, pp. 2577–2588, Nov. 2006.

[9] Z. Guo, A. Carlson, P. Liang-Teck, K. T. Duong, K. L. Tsu-Jae, and B. Nikolic, "Large-scale SRAM variability characterization in 45 nm CMOS," IEEE J. Solid-State Circuits, vol. 44, no. 11, pp. 3714–3192, Nov. 2009.

[10] Z. Guo, A. Carlson, P. Liang-Teck, K. T. Duong, K. L. Tsu-Jae, and B. Nikolic, "Large-scale read/write margin measurement in 45 nm CMOS SRAM arrays," in Proc. Symp. VLSI Circuits Dig. Conf., Jun. 2008, pp. 42–43.