DESIGN LOW POWER NETWORK ON CHIP (NOC) USING DATA ENCODING TECHNIQUES

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Abstract

A contrast of NOC's structure makes a fitting replacement for SOC design in designs incorporating large number of processing cores. In NOC the overall power dissipation is due to the interconnection system. The interconnects have become main element in dynamic power dissipation in a NOC design. The idea presented in this paper exploits the wormhole switching techniques and works on an end to end basis.That is flits are encoded by the NI before they are injected in the network and are decoded by the destination NI. In such a way as to minimize both switching activity and the coupling switching activity which represent the main factors of power dissipation. The data encoding technique in which number of switching transitions in data word is brought down to reduce the power dissipation. To verify the efficiency of the proposed technique, encoder and decoder structures are designed by using VHDL. As result, we obtain a reduction n total power dissipation and energy consumption up to 50% and 18%.

Index terms--- Network on chip(NOC), data encoding, wormhole switching power analysis, VHDL power analysis

I. Introduction

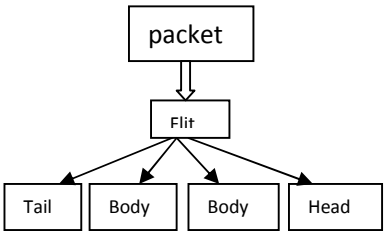
A network on chip communication gives flexibility in the topology , in support to that the flow control ,advance routing algorithms , self switching techniques guarantying the quality of service. A network on chip is an approach to design the communication subsystem between intellectual property cores in an system on chip [2]. In SOC. The SOC contains hundreds or thousands of cores and also the design complexity increases. In SOC the total length of the interconnection wire increases; resulting in long transmission delay. Such problem is minimized in NOC's [1].

NOC links can reduce the complexity of designing wires for predictable speed,power, noise, reliability etc.The wires in the links of NOC are shared by many signals. A high level of parallism is achieved because all links in the NOC can operate simultaneously on different data packets ,as the complexity of integrated systems keeps growing, NOC provides enhanced performance such as throughput and scalability in comparison with previous communication architecture such as SOC[3]. But power consumption is a key issue in NOC.

The basic elements which forms a NOC based interconnect are network interface routers and links. As technology shrinks, the power dissipation by the link is relevant as that dissipated by network interfaces. Links dissipate the power due to switching activity by means data encoding schemes [5]. The data encoding scheme proposed in this paper, is designed to exploit the wormhole switching technique.

Because of these advantages, namely better performance, small buffering requirements and greater throughput. Wormhole switching is a network flow control mechanism in that a packet split into one or more flits. A flit is a smallest unit on which flow control is performed. The result in that the flit of the packet are delivered in a pipeline fashion for the same amount of storage, it achieves lower latency and greater throughput [2].

The rest of the paper organized as follows –In section II The overview of proposal is discussed.In section III the existing system design is discussed. In the section IV encoding technique incorporated for power reduction is discussed. The working block of the encoder and decoder is discussed in the section V. In section V the simulation result is there.



II OVERVIEW OF PROPOSAL

The general scheme of proposed work is given in [fig.(1)]. The basic concept apply the encoding technique is end to end process. In end to end process the NI[4] augmented with an encoder[E] and decoder[D] block.

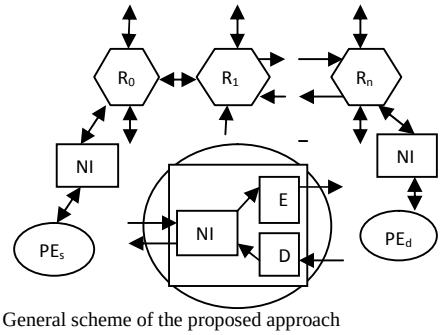


Fig.1. General scheme of the proposed approach

The most suitable switching techniques for on chip communication is wormhole switching. The pipeline nature is the basic concept for the wormhole switching. In wormhole switching the packet is converted into number of flits. The flits delivered in a pipeline as shown in [fig.(.2)]. The flit has head, body and tail. The header flit contains control information (destination address, packet size). With the exception of the header flits, the encoder encodes the out going flits in such a way as to minimize the power dissipation. Since the routers are not equipped with any encoding logic. The links of the routing paths are cross by the same sequences of flit, the encoding scheme ensure the same switching behaviour in each routing path [2].

In this proposed scheme we design our system with the help of digital representation.While the design of existing system,it requires more number of gates and couple of multiplexer compare with the proposed system. In proposed system the t_y block has couple of EX-OR gate and the majority voter block has one EX-OR gate. It leads to the reduction of power dissipation.

Fig.2.Flits delivered in a pipeline

III.EXISTING SYSTEM

The existing system operation based on EXOR , EX-NOR and multiplexer shown in [fig(3)]. When the current and previous encoded inputs are fed into the gates, the operation is taken into an account. The corresponding output W_1,W_2,W_3 and W_4 are given to the input of multiplexer. Then the output is given to the AND gate and also selection line output is fed into the EXOR gate. The finalized output is taken from the AND gate. This system required more power for gates and links. This hungry power is reduced by the use of proposed scheme which leads to reduce the power dissipation.

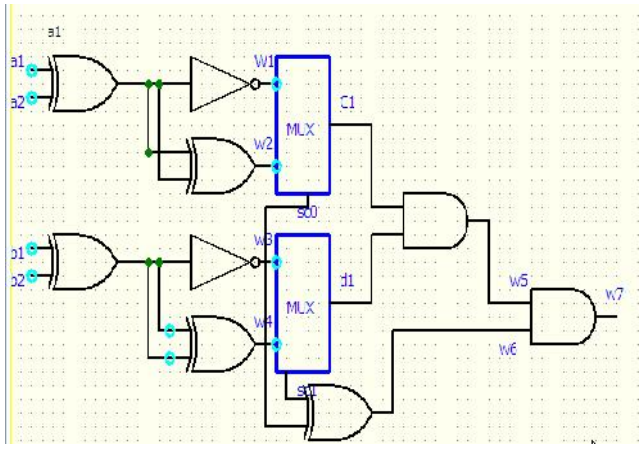


Fig .3.digital representation of existing system

IV.PROPOSED ENCODING SCHEME

In this section we present the proposed encoding scheme whose goal is to reduce power dissipation by minimizing the coupling transition activity on the links of the inter connection network. There are three types of encoding schemes. In scheme I we focus on reducing type I transition while in scheme II both type I and type II transition are taken into account. Finally in scheme III we consider the fact that type I transition show different behavior in case of odd and even inverts.

In this paper we present only scheme I, for reducing the number of type I transition (by converting them to type III and type IV transition) and type II transition (by converting them to type I transition). The scheme decide whether odd inversion or no inversion of the input data lead to the link power dissipation.

A type I transition occurs when one of the lines switches while the others stays unchanged. In a type II transition one line switch as from low to high and the other from high to low. A type III transition occurs when both lines switch simultaneously, finally in a type IV transition both lines do not switch [6]. Effort of odd inversion on change of transition type is given in (table 1).

Time	Normal Type 1			Odd Inverted types II, III and IV		
t-1 t	00,11,10,01 T1	00,11,01, 10,01,10, 00,11 T1**	01,10,11,00 T1***	00,11,11,00 Type III	00,11,01, 10,00,11, 01,10 Type IV	01,10, 10,01, Type II
t-1 t	01,10,10,01 Type II			01,10,11,00 Type1		

Table1 Effect of odd inversion on change of transition type

A.power model

The power model contains different components of power dissipation of a link. The dynamic power consumed by the inter connects and driver is given by

$$P=[T_{0->1}(C_s+C_l)+T_c+C_c]V_{dd}^2F_{ck} \rightarrow (1)$$

Where V_{dd} is the supply voltage, F_{ck} is the clock frequency, C_s is the self capacitance, C_l is the load capacitance, C_c is the coupling capacitance, $T_{0->1}$ and T_c are the average number of effective transition per cycles are C_s and C_c respectively

The coupling transition cavity T_c is a weighted sum of the different type of coupling transition contributions. Therefore

$$T_c=K_1T_1+K_2T_2+K3T3+K_4T_4 \rightarrow (2)$$

Where T_i , i=1,2,3,4……are the average number of transition type I, K_i are weights. According to [6] ,we assume $K_1=1$,$K_2=2$,$K_3=K_4=0$. K_1 is assumed as reference paper for other type of transitions. The effective capacitance in typeII transition is usually twice as that of type I transition. In type III transition both signals switch simultaneously C_c is not charged(here we assume that there is no misalignment between the two transitions). Finally , in type IV transition there is no dynamic charge distribution over C_c. so the equation(2) becomes

$T_c=T_1+2T_2$ → (3)

Substitute (3) in (1)

$P=[T_0->1(C_s+C_l)+(T_1+2T_2)C_c]V_{dd}^2F_{ck}$ → (4)

According to [6] C_l can be neglected

$P=[T_0->1C_s+(T_1+2T_2)C_c]$ → (5)

According to [1], $T_y>(w-1)/2$ → (6)

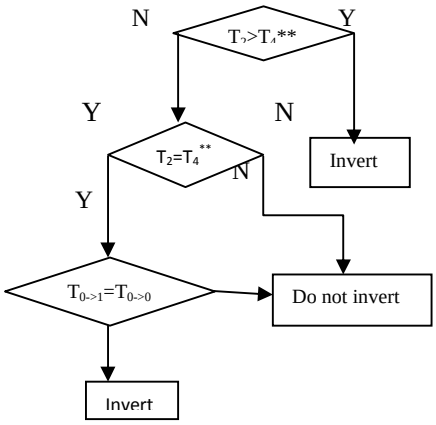
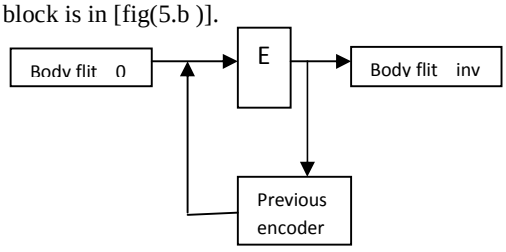


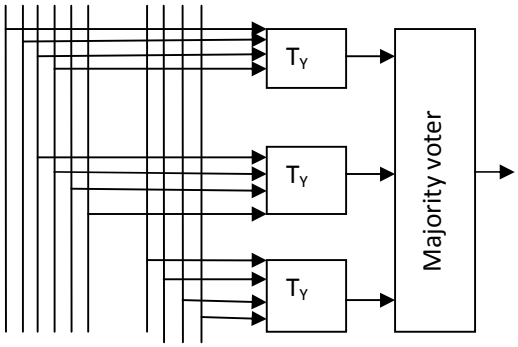
Fig.4. Flow chart to evaluate the invert condition

B.Design of encoder architecture

The proposed encoding architecture[fig (5.a)],based on odd invert condition Let us consider with links with of W bits. The NI packs body flits in W-1 bits. The W-1 bits body flit is concatenated with a'0' bit and it is represents the first input if the encoder. The second input is the previously encoded body flit[1]. The internal logic of the encoder block is in [fig(5.b)].



(a)



(b)

X_0 X_1 X_2 X_{W-2} X_{W-1}=0 (a)

Y_0 Y_1 Y_2 Y_{W-2} Y_{W-1}=INV (b)

(b)

Fig .5. (a)Encoder circuit diagram. (b) internal view of encoder block

This present the condition used to determine wheather the odd inversion to be performed or not. According to [1] we obtain the invert condition:

$T_{0->1}+8T_2>T_{0->0}+8T_4$-----→(7)

Looking at the invert condition (7) and considering a link with less than or equal to 8 bit.If T_2 is greater than T_4^{**}. Then the invert condition is satisfied [7], Based on flow chart shown in [fig.(4)].

To make the decision the previously encoded flit is compared with the current flit being transmitted. The W-1 bit of the incoming body flits are indicated by X_i [Y_i], Y=0,1,2……w-2. The W bit of the previous encoded body flit is indicated by inv, which shows if it was inverted [inv=1] or left as it was [inv=0]. In encoding , T_y blocks takes the two adjacent bits of the input flits and sets its output to'1'. If any of the transition types of T_y is detected. It leads to the reduction of power dissipation.

In this paper we designed the logic encoder architecture upto majority voter block. The result of the majority voter block is shown in [fig(6)]. For forth coming days we design the remaining stages of encoder block. if the condition given in (6) is satisfied (a higher number of 1's in the input of the block compared to 0's), then the inversion is performed on odd bits.

Result

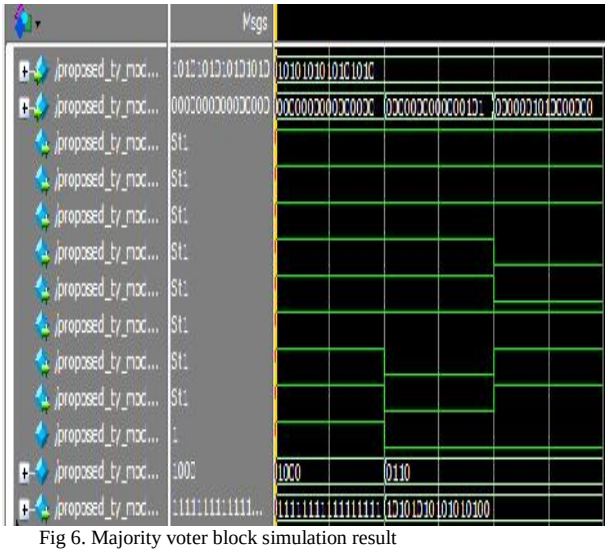


Fig 6. Majority voter block simulation result

Conclusion

In this paper we present Data Encoding Schemes aimed at reducing the power dissipated by the links of an NOC. As compared to existing method, the proposed schemes used less number of gates and links. It leads to reduce the power dissipation.

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