Latency reduction & increase in speed of Network on chip with a Four port router in a network

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ABSTRACT: **In this paper we mainly focused on four port router and here we design the verifies the functionality of the five port router for network on chip verify based on the latest verification methodologies, here we analysis the Hardware Verification Languages and EDA tools the Design for Synthesis and implementation. In this project we attempt to give a networking solution by applying VLSI architecture techniques to router design for networking systems to provide intelligent control over the network. Each router builds up a table listing the preferred routes between any two systems on the interconnected networks. When multiple routers are used in networks which are interconnected, the information is exchanged by the routers about destination address by using the dynamic routing protocol**.

I. Introduction

The router used here is it avoid congestion and communication bottleneck. Although there are number of router implementation had done previously. A few similar works are included here.Marescaux presented the implementation of router for NOC based system which has 2D torus network topology. Packet size was 8 bits and 2 control bits. The main drawback here was it was a 2D torus formed using 1D router which creates a serious bottleneck in traffic. Zerferino presented a soft core NOC router, which describes the problem for implementing the router by using an 8 flit buffer having 8 bit implementation which is relatively high. Its input and output channel has four distinct blocks and uses a larger logical decoding. Moraes further more turned-out its work on the other hand the disadvantage with it was that its packet has two headers which is relatively expensive. The buffer is present only with the input channel.[2] The testing for NOC requires more issues which covers fault coverage, detecting ability and locate faults, and designing the fault-tolerant network.

Multiple routers are used in interconnected networks and it exchange information about destination addresses by dynamic routing protocol. Each router builds table listing between any two systems in interconnected networks. It contains firmware for different networking protocols. Each network interface uses specialized software to enable data packets forwarded from one protocol system to another. Routers used to connect two or more logical groups of computer devices called subnets, containing different sub-network address. The subnet addresses placed in the router does not map to the physical interface.

OVM (open verification methodology) is an efficient methodology and it is free. This OVM is used effectively to achieve maintainability, reusability, speed of verifying capability and so on. This project is based to build the ecological test bench for verifying using system Verilog and OVM.

In this document the use of vmm and system Verilog to verify a design and to develop a reusable test bench is explained in step by step as defined by verification principles and methodology. The test bench contains different components and each component is again composed of subcomponents, these components and subcomponents can be reused for the future projects as long as the interface is same.

Problem Statement:

NOC technology is often called to be a front-end solution to the back-end problem. As a semiconductor transistor dimensions might shrink and increasing amount of IP block functions are added to the chip, also the physical infrastructure that carries data on the chip and then guarantees quality service to crumble.The existing method which uses resonant clocking, may increase the latency and throughput also decreased[1]. Considering this problem the project arose to make the proposed system more convenient. The project uses a four port router with 8 bit register and finite state machine with FIFO

II. Router

The communication on network on chip is carried out by the router for implementing better NOC, hence it should be designed economic. It ropes four parallel connections at the

same time. It uses store and the forward type flow control and FSM Controller deterministic routing which improve performance of the router. The switching mechanism of packet switching which is regularly used on network on chip [5].

Hence in packet switching the data transfers in the form of packets in between cooperating routers and independent routing decision are taken. The store with forward flow mechanism is considered to be best, because it does not reserve channels and thus does not lead to idle physical channels. Then the arbiter is of rotating priority scheme so that each channel get chance to transfer its data. The router containing both input and output buffering is used, so that blockage can be avoided at both sides.

A router is a device that forwards data packets across computer networks. Routers perform the data "traffic direction" functions with the internet. Hence router is a microprocessor-controlled device which is connected with two or more data lines comes from various networks. When a data packet comes from one of the lines, it reads the address information in the packet for determining its final destination,after using the information in routing table by directing the packet to the next network on its journey

A. The Proposed Router Architecture:

The Four Router Design is done by using three blocks .They are 8-Bit Register, Router controller and the output block. Hence the router controller architecture is designed by using FSM design and the output block consists of three fifo's combined together the fifo's are store packet of data and when u want to data that time the data read from the FIFO's. In this router design has three outputs that is 8-Bit size and one 8_bit data port it using to drive the data into router we are using the global clock and reset signals, and the err signal and suspended data signals are output's of the router[5] .The FSM controller gives the err and suspended data in signals .this functions are discussed clearly in below FSM description.

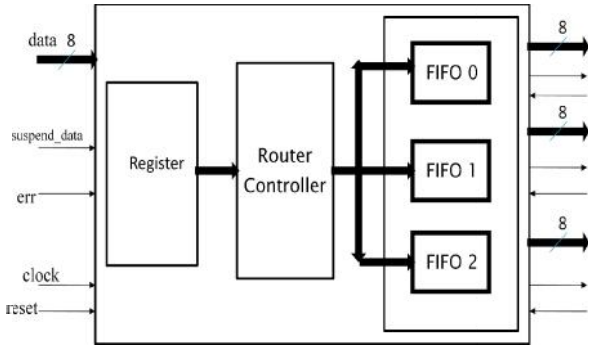

Figure1.1 - Four Port Router Architecture

The router_reg module contains the status, data and parity registers for the Network router_1x7.These registers are latched to new status or input data through the control signals provided by the fsm_router.There are 7 FIFO for each output port, which stores the data coming from input port based on the control signals provided by fsm_router module. Now a days , (NOCs) have been used in chip multi-processors (CMPs) to connect a number of processors[4].

The fsm router block provides the control signals to the FIFO, and router reg module. The Router blocks Diagram shown below fig.

Router blocks are

- Register
- Router controller(FSM)
- FIFO Output Block

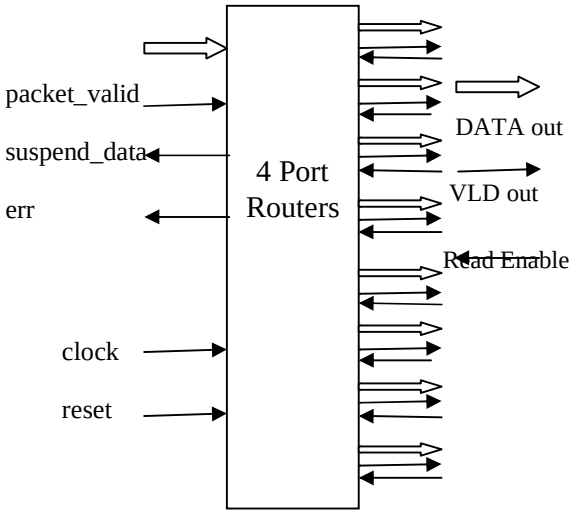

Fig 1.2 : Block Diagram Of 4 Port Router

B. Data Packet Format

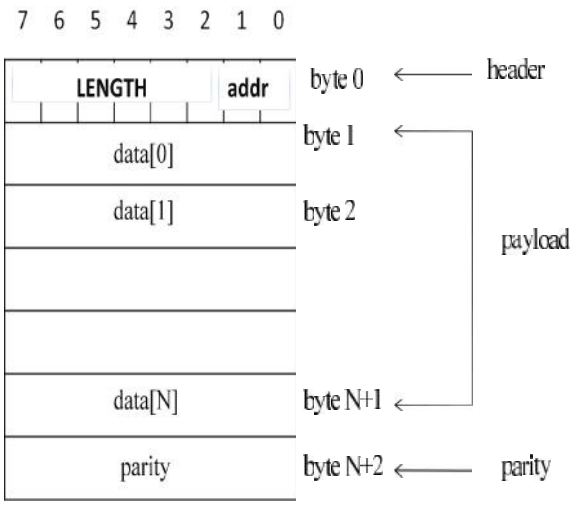

Fig 1.3: Format of Data Packet

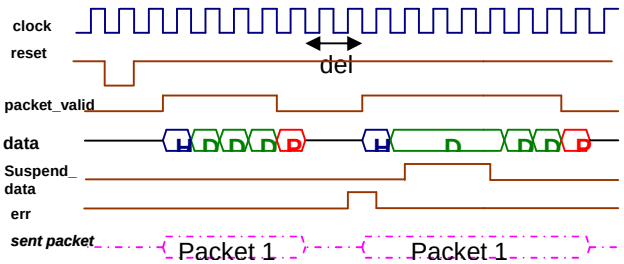

Fig: 2.1 Router Input Protocol

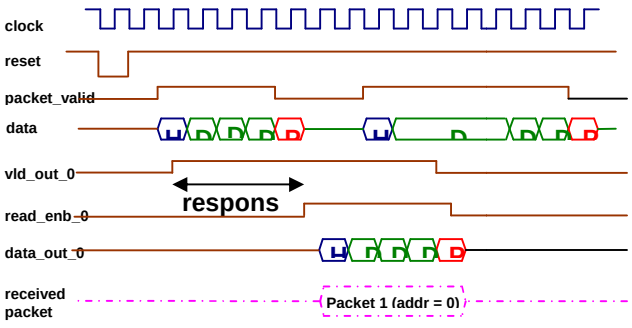

Fig: 2.2 Router output Protocol

III.Register Block

This module contains status, data and parity registers required by router. All the registers in this module are latched on rising edge of the clock.

Data registers latches the data from data input based on state and status control signals, in addition latched data is sent to the FIFO for storage. Also the data is latched into the parity registers for parity calculation and it is compared with the parity byte of the packet. By this an error signal is also generated whereas the packet parity is not equal to the calculated parity. [3]It must be noted that when this is applicable to 2D routers, it can be easily expanded to higher radix architectures.

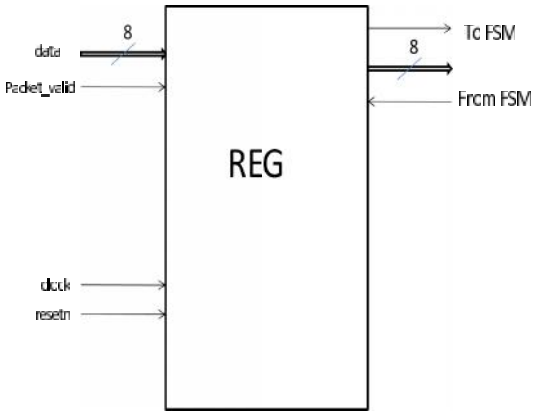

Fig 3.1: Register Block

IV. FSM Controller

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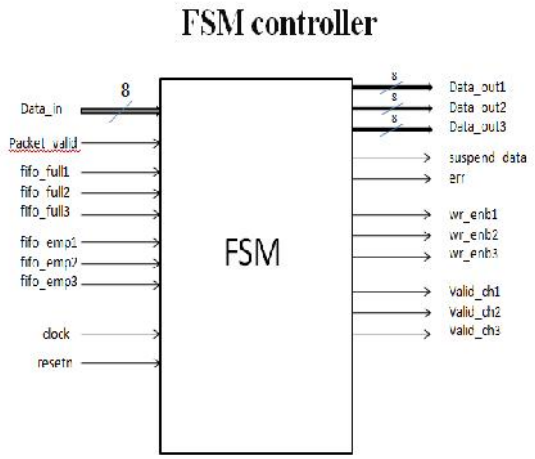

Input data is sent to FSM controller along with packet valid signal. And it decodes the address of the channel to which the data is to be sent.

By checking the status of the FIFOs it loads the data to the respective one. Then it suspends the data if the fifo is not empty or when the fifo is full and it checks the parity matching and generates error signal if any mismatches occur.

V.Router Output Block

There are 7 fifos used in the router design. Hence each fifo has 8 bit width and 16 bit depth.

The FIFO works on system clock. It has synchronous input signal reset. If resetn is low then full =0, empty = 1 and data_out = 0[1]

The FIFO performs 7 different types of operations

- Write Operation
- Read operation
- Read and Write Operation

The functionality of FIFO explain below,

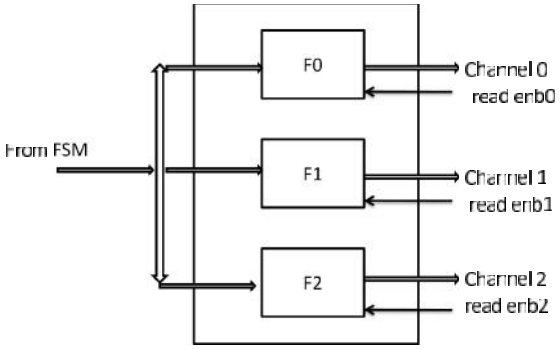

Fig:5.1 Four port Router FIFO

A.Write operation:

The FIFO write operation is done by when the data from input data_in is sampled at rising edge of the clock when input write_enb is high and FIFO is not full.from this condition only FIFO Write operation is done.

B.Read Operation:

The FIFO Read Operation is the data is read from output data_out at rising edge of the clock, when read_enb is high and fifo is not empty.

Read and Write operation can be done simultaneously.

Full – it indicates all the locations of FIFO are to be written.

Empty – it indicates that all the locations of FIFO are empty.

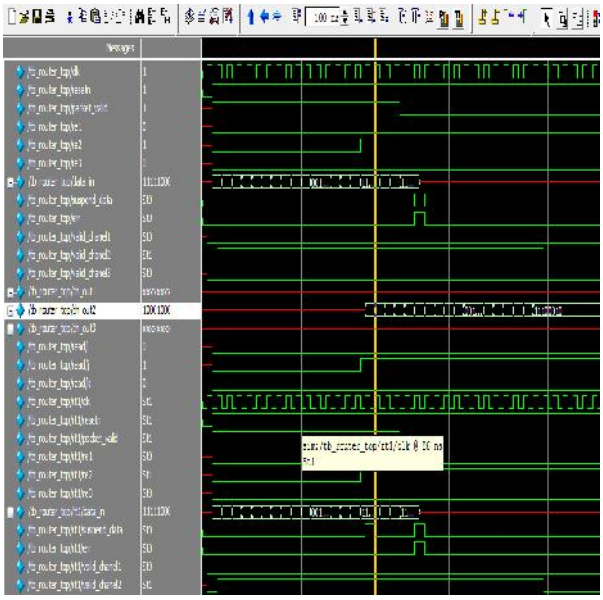

Fig 5.2 : Four Port Router Output

VI. Conclusion

In this Four Port Router project I Design and verified the functionality of Router with the latest Verification methodology System Verilog and observed the code coverage and functional coverage of Router by using cover points, cross and different test cases like constrained, weighted and directed test cases. By using these test cases I improved the functional coverage of Router. In this I used one master and eight slaves to monitor the Router. Thus the functional coverage of Router was improved and then its, better contention latency, bandwidth.

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