A PARADIGM OF REDUCING THE TRANSISTORS IN LOW POWER PULSE TRIGGERED FLIP FLOPS

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ABSTRACT: Low power has emerged as a principle idea in today's electronic industries. The power pulse triggered Flip-flop has various strategies for designing a low power circuits and systems. In this method, an explicit type triggered structure and a modified true single phase clock latch based on a signal-feed through scheme is implemented. The proposed design adopts a signal-feed through technique to improve the delay. The design also employs a static latch structure and a conditional discharge scheme to avoid superfluous switching at the internal node. This system also deals in solving a long discharging path problem in conventional explicit type pulse-triggered FF [1]. Here the operation is meant as when a clock pulse enters and if there is no data transition occurs, i.e, the input data and node Q are at the same level, then current passes through the pass transistor, which keeps the input stage of the FF from any driving effort.

Key words: pulse triggering

I.INTRODUCTION:

Flip-flops (FFs) are the basic storage elements used widely in all sorts of digital schematic designs. In particular, digital designs now-a-days often adopt intensive pipelining architecture techniques and employ many FF-rich modules. It is also estimated that the power analysis of the clock system, which consists of clock distribution network system and storage elements, is as high as 20%–45% of the total system power. Traditional master-slave flip-flops are made up of two stages, master and slave and they are formed by their hard- edge property. on the other hand , pulse-triggered flip-flops decrease the two stages into one stage and are characterized by the soft edge property[1]. Pulse-triggered FF (P-FF) has been considered a popular replacement to the conventional master–slave based FF in the applications of high-speed operations. Moreover the speed advantage, its circuits simplicity is also advantageous to lowering the power consumption of the clock tree system[4]. The circuit difficulty of a P-FF is simplified since only one latch, as opposed to two used in conventional master–slave configuration, is needed. P-FFs also allow time lent across clock cycle boundaries and feature a zero or even negative setup time. Subjecting on the method of pulse generation, P-FF designs can be classified as implicit or explicit[4]. In an implicit-type P-FF, the pulse generator is a built-in logic of the latch design and no explicit pulse signals are generated. In an explicit-type PFF, the designs of pulse generator and latch are different. Implicit pulse generation is often considered to be more power efficient than explicit pulse generation. In this paper, we are presenting a new concept of implicit P-FF with reduced number of transistors which will reduce the overall power area as well as delay.

II. PULSE TRIGGERED FLIP-FLOP:

The term pulse-triggered means that data are entered into the flip-flop on the rising edge of the clock pulse, but the output does not immitate the input state until the falling edge of the clock pulse. As this kind of flip-flops are susceptive to any change of the input levels during the clock pulse is still HIGH, the inputs must be set up before the clock pulse's rising edge and must not be changed before the falling edge. If not, ambiguous results will happen. The three basic types of pulse-triggered flip-flops are S-R, J-K and D[5]. The pulse triggered flip-flop having the low noise and low power switching activity[1].

The truth tables for the above pulse-triggered flip-flops are all the same as that for the edge-triggered

flip-flops, with the exception for the way they are clocked. These flip-flops are also called Master-Slave flip-flops simply because their internal construction is divided into two sections. The slave section is essentially the same as the master section except that it is clocked on the inverted clock pulse and is controlled by the outputs of the master section rather than by the external inputs. The data lock-out flip-flop is similar to the pulse-triggered (master-slave) flip-flop except it has a dynamic clock input[8]. The dynamic clock disables (locks out) the data inputs after the rising edge of the clock pulse[8].

III. PROPOSED SYSTEM:

This P-FF adopts two measures to overcome the problems combined with existing P-FF designs. The first one is reducing the number of NMOS transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when the input data is "1." As opposed to the transistor stacking design transistor N2 is removed from the discharging path[8][7][2].

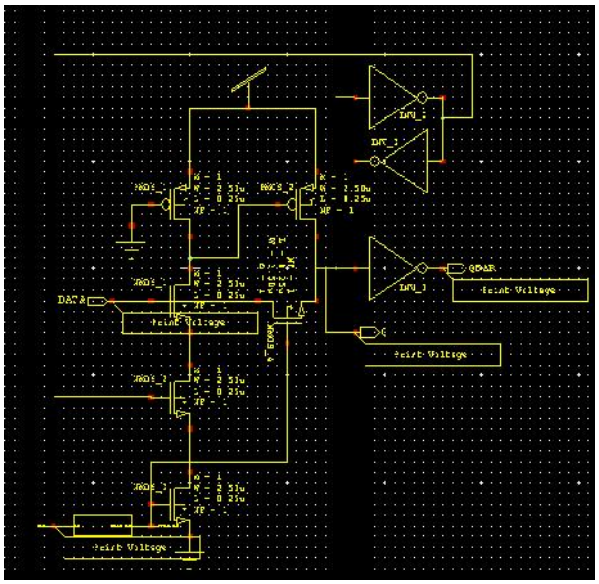

Fig. 1

Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. In this proposed P-FF the load capacitance has been reduced and the ground bounce noise to be reduced. The pass transistor has been to be added in the circuit to controlled by the pulse clock signal to reduce the switching power. The pull up and the pull down transistor also to be enable the clock pulses for the input of the data and the clock[8]. This scheme actually improves the "0" to "1" delay and thus reduces the disparity between the rise time and the fall time delays. Reduces the time and the switching delay automatically reduces the switching power proposed in the circuit[6].

IV.RESULT AND ANALYSIS:

Schematic function

In these figures below we considering based on 4 NMOS transistor and 2 PMOS transistor supply voltage will be given to the data node and it will act as input node and output node is Q and Qbar .5 v supply will be given to the schematic circuit .the circuit schematic based on 90nm technology

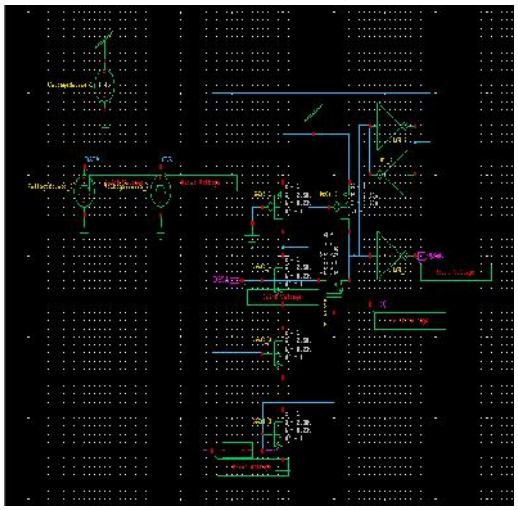

Fig 2

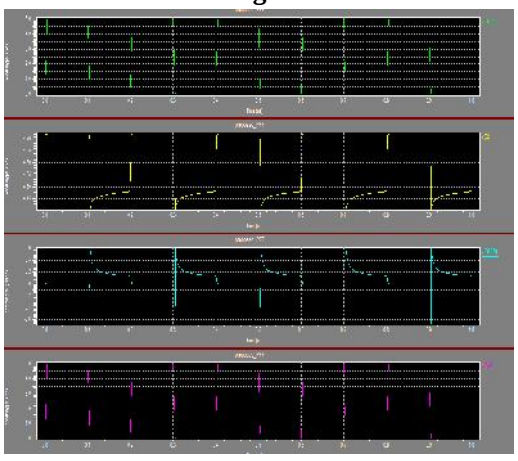

Fig.3

COMPARISION TABLE:

FACTORS ANALYSIS	EXITING	PROPOSED
Power(μW)	**0.300**	**0.258**
transistor	**24**	**12**
Computational time	**1.42S**	**1.36S**
technology	**90nm**	**90nm**

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V.CONCLUSION:

The pulse triggered flip flop using signal feed through scheme is used to design parallel counter. The universal shift registers are designed existing and proposed pulse triggered flip flop and parallel counter designed using CMOS design with nanometer Technology to achieve low power, less delay and power delay[3][6]. In this Paper we proposed a new pulse triggering flip flop design which has only 9 transistors, show much power less and Area constraints than the other existing Flip-Flop designs[2]. As well as the design will be having very less clock delay when compared to other circuits. Thus our proposed system is having less power and area constraints.

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