AN EFFICIENT HYBRID EVOLUTIONARY ALGORITHM FOR VLSI CIRCUIT PARTITIONING

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ABSTRACT: **VLSI Physical design plays a vital role in designing the Integrated Circuits in order to reduce the complexity. In physical design, Partitioning is an important step hierarchical, building-block design methodology. The main objective is to optimize the interconnections between the circuits. To meet the above objective, we propose Bi-partitioning technique to divide the circuit into sub-circuits. To achieve the optimized net-cuts, hybrid evolutionary algorithm is applied with the consistence of Genetic algorithm (GA) and modification Fiduccia-Mattheyses (FM) algorithm. Initially GA is used as global search procedure and later modified FM algorithm is used as local search procedure to get the optimized solution. The net list information of the circuit has been retrieved from the ISPD'98 circuit benchmark suite.**

Keywords: Partitioning, net list optimization, hybrid evolutionary algorithm, local search.

1. INTRODUCTION:

As the VLSI design complexity increases it leads to more integration, increase in design size, in interconnects and in delay. To handle these issues, circuit partitioning plays an important role in VLSI physical design by dividing the circuit into the sub-circuits. The main objectives of VLSI circuit partitioning are:

1. To minimize the number of interconnections between the partitioned sub-circuits: it not only reduces the delay but also reduces the interface between the partitions [6].
2. To minimize the delay due to interconnections: if the delay between the partitions is larger than the delay within the partitions, it is an important consideration in circuit partitioning [10].
3. Ratio-cut minimization: the limitation of number of terminals is decided by the number of terminals of sub-circuits [6].
4. Maintain the area and number of partition within specified bounds: to ease the design, reduced cost with minimum area and increased cost with more number of partitions are used as constraints [10].

To solve the partitioning problem in an efficient way the circuit is converted into graph. The max-bisection problem, partitioning the vertices of a graph into two equally sized subsets and it is a NP-hard combinatorial optimization problem [4]. Problems in NP-hard do not have elements of NP indeed they may not even be decision problems. Combinatorial optimization is a subset of mathematical optimization related to operation research, algorithm theory and computational complexity theory.

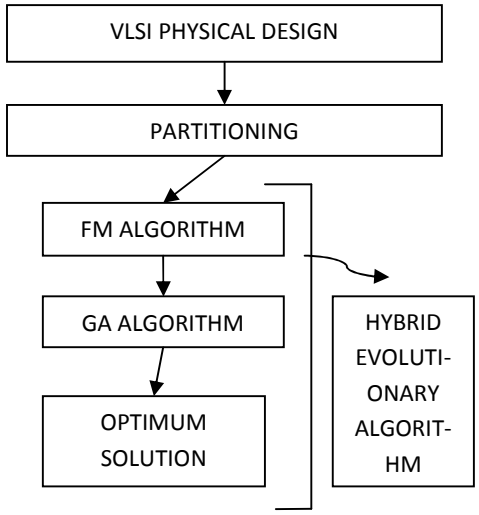

Fig 1: Proposed VLSI partitioning process

In this paper, we propose a memetic algorithm (MAMB) for the max-bisection problem. Our MAMB adopts a local search procedure (FMMB) to quickly improve the quality of each initial solution in the population n. Based on the solution representation and the characteristics of the max-bisection problem, a cross-over operator is designed to generate an offspring, which is then refined by the FMMB further [1].

Let G= (V, E) be an undirected graph with a vertex set V= {1, 2, n} and an edge set E with weights $w_i \geq 0$ for each {i, j} €E. we denote the number of vertices by n and number of edges by m [1].

The rest of the paper is organized as follows: the following section presents the details about partitioning such

as problems in partitioning, I/O file, and so on. The problem is formulated in section 2. The proposed graphical method is discussed in section 3. FM algorithm and its steps are presented in section 4. Genetic Algorithm, its methods and its steps are provided in section 5. Conclusion of this paper is given in section 6.

2. PROBLEM FORMULATION

Circuit partitioning divides a circuit into smaller sub circuits in order to minimize the number of connections between the sub circuits. The partitioning problem can be solved by following techniques: 1.clustering 2. Graph3. Ratio cut 4. Stochastic algorithms 5. Neural algorithms [7]. Here the circuit is represented as graph. In this graphical representation, each node represents a physical component such as gate, adder, etc., and each edge represents a physical connection between two components [2].

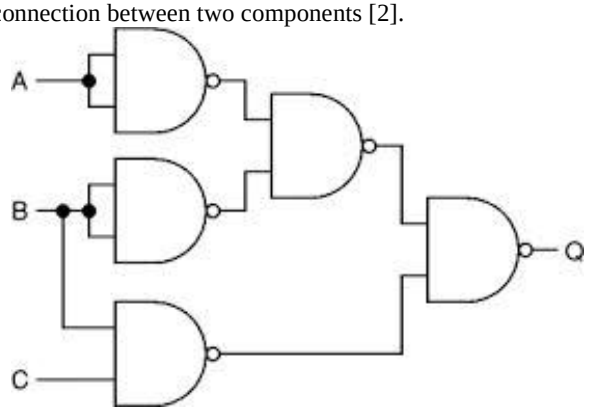

Fig 2: Logical circuit

Input to our program is the net lists, pin location and area of the given standard circuit. Output is the minimized net lists between bi-partitioned sub circuits [3].

Input file:

Circuit- nets: including name and quantity of nets, interconnections with standard cells and obstacles and connected pin locations.

Output file:

Design- Nets: the result of standard circuit's minimized net list.

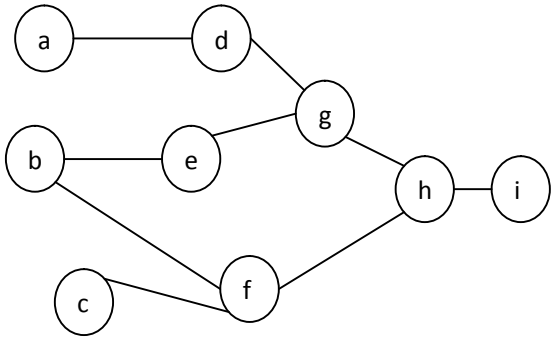

Fig 3: Graphical representation of the logical circuit

Objective:

The interconnection between the sub-circuits is minimized by using the Genetic algorithm and modified FM algorithm.

3. PROPOSED DESIGN

The given standard circuit is converted into graphical representation.

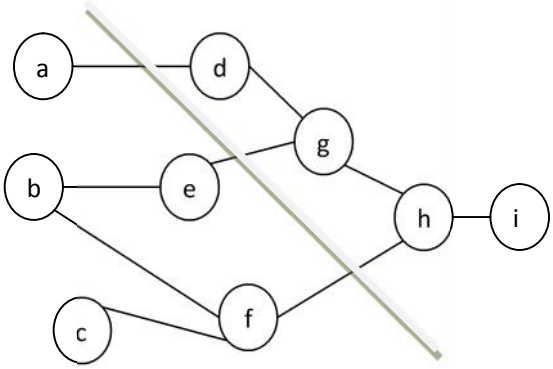

Fig 4: Bi-partitioning of a graph

This graph is then bi-partitioned to get the minimized interconnections between two sub-graphs by using Genetic algorithm and later the modified FM algorithm as local search procedure is used to get the optimized solution. The quality of the final partition depends on the initial partition [7].

In Fig 4, a graph G (V, E) = G (9, 9) is partitioned into two sub-graphs. The vertices V of the graph is represented by numbers and the edges E are represented by straight lines. In circuit representation of the graph the vertices are considered as modules whereas the edges are considered as interconnections between the modules.

Number of vertices (modules) = 9

Number of edges (interconnections) = 9

The benchmark from which the circuit information retrieved is ISPD'98 benchmark. The circuit information is in the form of circuit netlists in accordance with the benchmark suit. Netlists can be considered as the hyper graph with modules as vertices and interconnections as edges.

4. GENETIC ALGORITHM

The Genetic algorithm is used as a global search procedure to reduce the netlist. To get the optimal solution is the main objective of Genetic algorithm. Since GA's are heuristic procedure, we can get good solutions for wide range problems but not optimum solution [10]. In Genetic algorithm, to get the optimum solution following steps are used: initial population, selection, cross over and mutation. Initially GA uses individuals as an initial population. GA selects the population based on their fitness to generate the optimum solution. Some of cross over techniques such as uniform crossover, one point crossover, two point crossover and so on, depending on the necessity. To maintain genetic diversity from one generation to another generation, mutation is performed.

4.1 Initial population

The initial population is randomly selected individuals. The creation of the initial population is finished when the fitness value is enough for next generation.

4.2 Selection

The selection process is based on fitness [11]. The individual which has higher fitness gets higher priority and the individual which has lower fitness gets lower priority. The higher fitness may be selected several times and the lower fitness should be discarding [10]. There are several types in selection: Roulette wheel selection, ranking and scaling selection and etc.

4.3 Crossover

The crossover in Genetic algorithm is used to create an offspring for the next generation. Crossover is the process of combining the bits of individuals. It randomly selects the bits and combines it to generate the new generation.

4.4 Mutation

To prevent all solutions in population, the mutation process is performed after crossover [11]. Mutation is flipping the bits from 0 to 1and from 1 to 0.

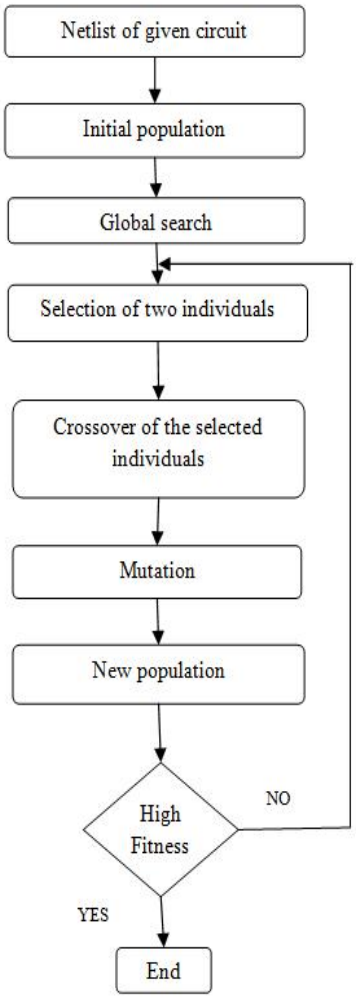

Fig 5: GA algorithm – Flow chart

If the fitness of the new population is low, then the GA process is repeated from the selection module to get the optimized solution for the VLSI partitioning netlist problem.

5. MODIFIED FM ALGORITHM

KL and FM are two well known iterative improvement algorithms for graph partition. They have been used as a constituent in many circuit partitioning algorithms and graph partitioning algorithms for getting high quality partitioning solutions. Our proposed local search algorithm FMMB uses the same iterative improvement framework as FM. Local search moves from one solution to another solution until an optimal solution founded [1].

FMMB Algorithm Steps:

Step 1: *Better feasible solutions are selected randomly from the GA algorithm as initial population for FMMB.*

Step 2: *Calculating the gain for various iterations of selected solutions.*

Step 3: *Update the gain and continue the iteration of the cells.*

Step 4: *The process ends when the balanced bi-partition with maximum gain is obtained.*

Since the time complexity of FM algorithm is less, the modified FM suggests that only one node must be moved at a time with consecutive manner in opposite direction [6]. So the algorithm runs much faster. This algorithm maintains the sorted list of candidate nodes and updates it after moves. A node may be a base node if that node doesn't violate balance criteria and maximizes the gain. The gain of node is the number of nets by which the cut set would decrease if a node moved.

6. CONCLUSION

Since the VLSI partitioning is NP-hard in combinatorial optimization problem, a hybrid evolutionary algorithm is developed to solve it in an efficient way. Here the Hybrid evolutionary algorithm consists of Genetic algorithm and modified Fiduccia-Mattheyses algorithm. Initially Genetic algorithm is implemented as global search by which two solutions are randomly selected as parent. The selected individual undergoes crossover and mutation to generate the offsprings as new solutions for partitioning problem. The modified Fiduccia-Mattheyses applied as local search procedure to VLSI circuit partitioning, produces optimized solution for netlist optimization problem. In this work, the algorithms are implemented by using MATLAB. To achieve a balance between intensification and diversification, the proposed algorithm integrates a new fast local search procedure, a pool updating and a crossover operator strategy.

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