DESIGN OF DRAM BASED FPGA

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Abstract- **As new nonvolatile memory technologies become increasingly mature, there has been a growing interest on investigating their use in field-programmable gate arrays (FPGAs). We can use these non-volatile memories in the future FPGA, instead of using embedded flash memory in the presently used FPGA, which can also store configuration data. First, we must identify a appropriate design for this new non-volatile configuration data storage memory. But the dynamic random-access memory (DRAM) based design strategy enabled only by high-density embedded non-volatile memory. The currently used FPGA do not uses on-chip DRAM cells for configuration data storage, because self-refreshing in DRAM involves destructive DRAM read. In order to solve this problem, we have planned to use embedded non-volatile memory as primary FPGA configuration data storage and externally refresh on-chip DRAM cells. To demonstrate the potential advantages of such a design strategy, the analysis and simulation are planned to be carried out.**

***Keywords*—Dynamic random-access memory (DRAM), field-programmable gate arrays (FPGA), magnetoresistive random-access memory (MRAM), nonvolatile memory.**

I.INTRODUCTION

Tthe semiconductor industry has experienced a resurgence of interest in the search for highly scalable memory technologies,over the years. Among various memory technologies, phase-change random-access memory (PCRAM) and magneto resistive random-access memory (MRAM) are the two most promising candidates and hence have received a lot of attention.

A.PHASE-CHANGE RANDOM ACCESS MEMORY(PCRAM):

Phase-change random access memory, PCRAM, is a form of non-volatile memory that is faster than Flash memory that was in widespread use.This form of memory may known by a number of names including phase change memory, PCM.Phase change memory, PCM will be based on a technique known as the memresitor that was initially developed by Hewlett Packard.Now PCM, phase change memory have been taken up by a number of other manufacturers including: Intel; Numonyx (now owned by Micron); Samsung; and others. Phase change memory is seen as a significant advance and one that was likely to become one of the mainstream formats for this semiconductor memory.

The phase change memory, PCM or phase change random access memory, P-RAM, exploits the a unique property of a substance known as chalcogenide glass.The PCRAM uses the fact that the chalcogenide glass changes between two states, polycrystalline and amorphous by the passage of current which produces heat as it passes through a cell. It gives rise to the name phase change, as the substance changes between the two phases.In the amorphous state the material demonstrates a high level of resistance and also a low reflectivity.In the polycrystalline state the material had a regular crystalline structure, and this manifests itself in a change of properties. In this state it had a low resistances as the electrons is easily able to move through the crystalline structure, and it is also exhibits the high reflectivity. For this phase change memory / phase change RAM, it will be the resistance level that will be of interest.

Circuitry around the cell will be then detects the change in resistance as the two states had a different resistance and as the result it detects whether a "1" or "0" was stored in that location.The phase change between the two states of the chalcogenide was brought about through localised heating brought about as the result of injected current for the timed period. The final phase of the material was modulated by the magnitude of the injected current and the time of the operation.A resistive element provides the heating and it extends from a bottom electrode to the chalcogenide layer. Current passing though this resistive heater element provides the heat which are then transferred to the chalcogenide layer.

B.ADVANTAGES OF PCRAM OVER FLASH MEMORY:

Non-volatile: Phase change RAM is the non-volatile form of memory, i.e. it does not require power to retain its own information. It enables this to compete directly with flash memory.

Bit alterable: Similar to RAM or EEPROM, PCRAM was what will be termed bit-alterable. It means that information can be written directly to this without the need for the erase process. It gives a significant advantage over flash which requires an erase cycle before the new data can be written to this.

Fast read performance: Phase change RAM, P-RAM features fast random access times. It had the advantage of that it enables the execution of code directly from the memory, without the need to copy the data to RAM. The read latency of P-RAM was comparable to single bit per cell NOR flash, while the read bandwidth was similar to that of DRAM.

C.MAGNETO-STATIC RANDOM ACCESS MEMORY(MRAM):

MRAM (magneto resistive random access memory) was the method of storing data bits using magnetic charges instead of the electrical charges used by DRAM (dynamic random access memory). Scientists define the metal as the magnetoresistive if this shows the slight change in the electrical resistance when placed in a magnetic field. By combining this high speed of static RAM and the high density of DRAM, which say MRAM would be used to significantly improve electronic products by storing greater amounts of data, enabling it to be accessed faster while consuming less battery power than existing electronic memory.Conventional random access memory computer chips store information as long as the electricity flows through them. Once the power was turned off, the information had lost unless it had been copied to the hard drive or floppy disk. MRAM, however, retains the data after a power supply was cut off. Replacing this DRAM with MRAM could prevent data loss and enable computers that start instantly, without waiting for software to boot up.

D.ADVANTAGES OF MRAM:

MRAM is a non-volatile memory storage system like Flash memory, but this uses much less power and switches significantly faster. The main advantage of this MRAM was that while Flash memory typically had the write time measured in milliseconds, MRAM had a write time measured in nanoseconds.

E.FIELD-PROGRAMMABLE GATE ARRAY :

A field-programmable gate array{FPGA) is an integrated circuit designed to be configured by the customer or a designer after manufacturing – hence it is known as "field-programmable". Contemporary FPGAs had the large resources of logic gates and RAM blocks to implement complex digital computations. As FPGA designs employ very fast I/Os and bidirectional data buses it becomes the challenge to verify correct timing of valid data within setup time and hold time.

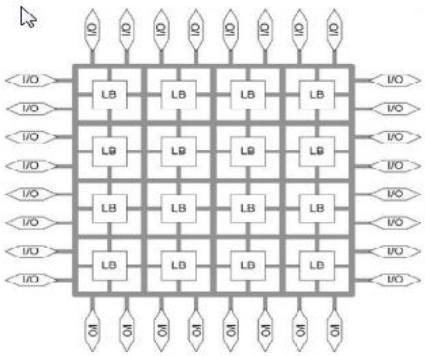


Fig (1).FPGA structure

Logic blocks can be configured to perform complex combinational functions, or merely simple logic gates like AND and XOR. In most FPGAs, the logic blocks also include memory elements, which may be the simple flip-flops or more complete blocks of the memory.FPGAs contain programmable logic components which are called "logic blocks", and a hierarchy of reconfigurable interconnects may allow the blocks to be "wired together" like many logic gates that can be inter-wired in many configurations.

F.RAM-BASED FPGA:

In this proposed algorithm, we have interested in exploring the potential of realizing the embedded nonvolatile configuration data storage for future field-programmable gate arrays. Most FPGAs use distributed on-chip static random-access memory (SRAM) cells to store the data for configuring both the logic components and interconnects, where configuration data are persistently stored off-chip and loaded to initialize on-chip SRAM cells during power-up. Flash memory has been used to realize nonvolatile FPGAs with two different design styles are distributed-embedded Flash memory cells can replace SRAM cells to store configuration data and configure logic components and interconnect,which is referred to as fully distributed design style in this brief and standard SRAM-based FPGAs were supplemented with one embedded Flash memory block that will stores the configuration data and initializes distributed SRAM cells during power-up, which is referred to as fully centralized design style in this brief.

Both PCRAM and MRAM can be achieve higher storage density and require fewer mask layers, when compared with this embedded Flash memory .With respect to using this emerging nonvolatile memory in FPGAs, prior work, focused on the fully distributed design style with the use of MRAM. Since PCRAM and MRAM realize data storage by which it modulating the resistance of each memory cell and full-swing voltage signals were required in FPGA configurations.

We have to convert this stored configuration data from resistance state to voltage level.Although this can be easily done within the context of a centralized memory block, when this fully distributed style was being used, such resistance-to-voltage conversion becomes nontrivial. As the result, prior work mainly focused on how to address such fully distributed resistance-to-voltage conversion issue. In each of the configuration bit was persistently stored in the pair of magnetic tunneling junctions (MTJs) that is programmed differentially, which was used to bias one SRAM cell that converts the differential resistance into a full-swing voltage signal.

After the conversion during power-up, each SRAM cell holds the configuration bit and configures the corresponding logic element or inter connect. Apparently, this design approach increases the area overhead for configuration data storage. Aiming that at reducing the area

overhead, the authors of proposed to use the pair of differential MTJs are used to form a voltage divider that will directly converts the configuration bit from resistance domain to voltage domain. To obtain this full swing voltage signal at minimal area overhead, architecture of FPGA logic elements was modified so that several MTJ-based voltage dividers can be share one SRAM cell.

Although such a fully distributed design style enables true instant-on FPGAs, it is subject to two major issues, one of the issue was due to the increasingly significant device variability and reduced allowable sensing current as these emerging memory technologies is being scaled down, there may not be sufficient operational margin to ensure reliable resistance-to-voltage conversion, especially when MTJs are directly used to build a voltage divider as in and another one issue is more importantly, those emerging memory technologies may suffer from relatively high defect density and/or write failure rate. However, such a fully distributed design style would not be able to use conventional memory fault tolerance techniques to handle the defects and write failures.

In this brief, we focus on the use of MRAM, and the design/evaluation strategy can be readily extended to the case of PCRAM. First, we have to use VPR to evaluate the area and speed performance of FPGAs with fully distributed MRAM memory cells, which is further compared with conventional SRAM-based FPGAs. When compared with its SRAM-based counterpart, such a fully distributed design approach may result in an area overhead of 14.4%.

We have very optimistically estimate MRAM cell size and ignore any possible memory cell defects, which is also leads to noticeable speed performance degradation. Next, we have to evaluate the fully centralized design approach, where a single embedded MRAM block is used to persistently store the configuration data and initialize the distributed SRAM cells during power-up. Even assuming the use of error correction codes for memory defect tolerance, this design approach only results in an area overhead of 7.9% and can maintain almost the same speed performance as conventional design practice.

Hence, the results suggest that while considering the inevitable significant process variability and non negligible defect densities of these emerging memory technologies, a fully centralized design style is more favorable. Moreover, we note that recent research demonstrated that such centralized design style can also effectively enable run-time dynamic re-configurability.

We propose a new design to replace the SRAM cells with dynamic random-access memory (DRAM) cells to reduce the area and use embedded MRAM to refresh DRAM cells, beyond simply replacing embedded Flash memory block in the centralized design style. We may also elaborate on the analysis of cost induced by periodic on-chip DRAM refresh. We further use the versatile place and route (VPR) tool set to quantitatively evaluate the involved tradeoffs and potential speed performance benefits. Through this detailed VERILOG simulations and VPR modeling, we show that, for a 45-nm FPGA consisting of 80×30 tiles, such a DRAM-based FPGA design strategy can reduce the FPGA die footprint by up to 8.4%, while its DRAM refresh power consumption was only up to 54.7 mW.

II.DRAM-BASED FPGA

Dynamic random access memory (DRAM) is the type of random-access memory used in computing devices (primarily PCs). DRAM stores each bit of data in a separate passive electronic component that is inside an integrated circuit board. Each electrical component has two states of value in one bit called 0 and 1. This captivator needs to be refreshed often otherwise information fades. DRAM has one capacitor and one transistor per bit as opposed to static random access memory(SRAM) that requires 6 transistors. The capacitors and transistors that are used are exceptionally small. There are millions of capacitors and transistors that fit on one single memory chip. However, the capacitors in DRAM need to constantly be refreshed to keep their charge.Compared with SRAM-based FPGAs, this DRAM-based FPGA design strategy can reduce the logic element and interconnect silicon area, leading to speed improvement. On the other hand, this design strategy is subject to certain implementation overheads. In particular, the periodic on-chip

DRAM cells refresh may incur no negligible extra energy consumption. Hence, the refresh circuits and energy cost must be carefully designed and analyzed. These overheads heavily depend on the retention time of on-chip DRAM cells, which further depends on the implementation of DRAM cells. The DRAM refresh power consumption is mainly dominated by the power consumed by bit-lines/word-lines, and the planar DRAM structure tends to have low retention time and hence high refresh frequency. Therefore, we may need to use a partially centralized style, in which the FPGA array is partitioned into several regions and each region has its own centralized MRAM block. This can readily accommodate the low retention time and meanwhile reduce refresh power consumption because of relatively shorter bit-lines/word-lines

A.ON-CHIP DRAM REFRESH COST ANALYSIS:

DRAM chip can hold more data than an SRAM (static RAM) chip of the same size can. However, the capacitors in DRAM need to constantly be refreshed to keep their charge, so DRAM requires more power than SRAM. The DRAM refresh power consumption is mainly dominated by the power consumed by bit-lines/word-lines, and the planar DRAM structure tends to have low retention

time and hence high refresh frequency

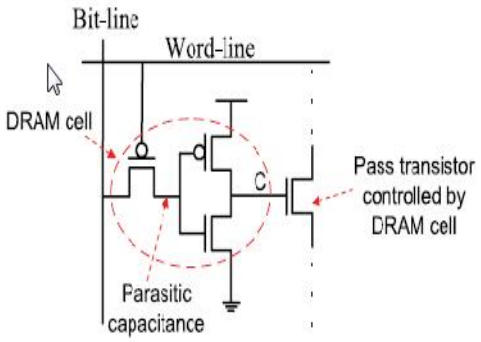


Fig.No.2. Illustration of on-chip planar DRAM cell structure based on parasitic capacitance

This can readily accommodate the low retention time and meanwhile reduce refresh power consumption because relatively shorter bit-lines/word-lines. In this specific case study, we set the nMOS transistor with minimum size, the pMOS transistor with 1.3 × minimum size , and the pMOS pass transistor with 4 × minimum size. Hence, according to the area estimation method used in VPR. Ineach DRAM cell has 4.65 minimum-width transistor size In this case study, by carrying mout further VERILOG simulations based on the above configurations, we set the DRAM cell retention time as 100 μs .

B.SIMULATION RESULT OF DRAM REFRESH POWER CONSUMPTION:

Simulations using the VPR tool set show that each FPGA tile contains 1176 DRAM cells, and each FPGA tile has the size of 66 µm × 66 µm. We put two buffers on each word-line and bit-line. We partition the entire FPGA die into two parts, and each part has its own embedded MRAM. Using the modified CACTI tool, we estimate that the MRAM read access latency and read energy consumption are 1.86 ns and 0.016 nJ per bit and refreshing each word-line takes Tcycle = 16.5 ns, leading to a total 45.4 µs for refreshing all the DRAM cells once. This can well satisfy the 100-µs DRAM cell retention time as estimated above. Assuming P0 and P1 are both 0.5, we estimate that a total 4.37 µJ (including energy consumed by word-lines/bit-lines and MRAM memory read) will be dissipated for refreshing all the DRAM cells once. Hence, assuming a DRAM refresh period of 80 µs, the overall DRAM refresh power consumption is 0.0547 W. Regarding the leakage energy consumed by the inverters within DRAM cells, as pointed out above, the static leakage current reaches 36 nA (denoted as Ileak1) and 450 pA (denoted as Ileak0) if its input voltage increases from 0 to 0.4 V or reduces from 1 to 0.81 V. From our VERILOG simulations, the inverter static leakage current increases approximately linearly as its input voltage changes.

III.EXISTING ALGORITHM

A.SRAM BASED FPGA:

FPGA stand for Field-Programmable Gate Array and is an integrated circuit that can be programmed after it was manufactured, hence its name “Field Programmable”. There are two different types of FPGAs, one that only can be programmed once called One-Time Programmable, OTP, and one that was reprogrammable. OTP technology was much more common in space qualified designs because it was in general more robust than the reprogrammable one.

But, the in-system re-programmability of FPGAs was of great importance giving extreme flexibility to the application, which can be updated in case of changing requirements or failure recovery. The issue was that the reprogrammable FPGA’s sensitivity to radiation, which had to be discussed more in detail in the next chapter. To be programmable a FPGA contains numerous configuration switches that after programming routes the different Logic Blocks, LB, together. A typical FPGA contains Logic Blocks that make up the bulk of the device and they had based on Lookup Tables, LUT, combined with one or two single-bit registers and additional logic elements such as clock enables and multiplexers.

These Logic Blocks and LUTs look differently depending on the technology used, different companies use different technologies, but it may usually also differ between product series within a company. These Logic Blocks are then connected through a grid surrounding them, which also connect with the I/O pinsat the edges.

Many FPGAs provide internal SRAMs located between the Logic Blocks to greatly improve functionality. This feature opens up to new possibilities although it also brings about another trait that is usually sensitive to radiation. But despite that the use of SRAM-based FPGA is growing in space based applications because of low application development cost, short time to market, and the reprogramming flexibility that they offer. The need is recognized and today there are FPGAs with radiation tolerant SRAM designs..

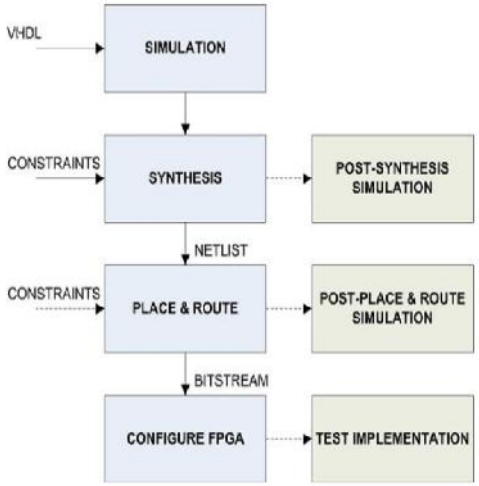


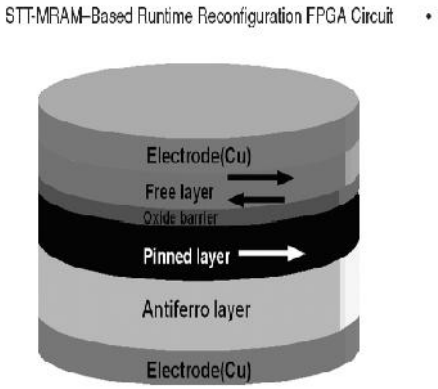
Fig (3).DESIGN FLOW

But these bring about even more radiation issues to overcome.The main objective of this project was to made a general assessment of the design kit AT40KEL -DK from ATMEL and the included FPGA, AT40KEL040. It was not only the hardware that was important to evaluate, it was also necessary to test the effectiveness and user friendliness of the belonging software as well. As the first stage of the FPGA will be tested by implementing a Space Wire-codec from University of Dundee, which will raise the level of this experience with the kit and in that way simplify further testing.

Problems that have been overlooked otherwise will emerge before the final testing plan was made for the additional tests. The goal has not to have a fully operational Sp W-node working at high speed, but to had the basic functionality at low speed. Different generated macros will also be created and stressed in several ways. The will both examine some of the specific technologies and test the macro generator software. The results are a good indicator of the performance and functionality of the design kit as well. A comparison can then also be made between identical functionalities not created by the macro generator.

B.MRAM BASED FPGA:

Magnetic RAM (MRAM) had been rapidly evaluated as one of the most promising spintronics applications. It represents advantages such as non-volatility, high write/read speed, limitless endurance, radiation hardness, and the like. The use of MgO barrier in the Magnetic Tunnel Junction, basic memory cell of MRAM, improves significantly the tunnel magneto-resistance (TMR) effect and has its reading performance. Furthermore, the development of novel writing approach based on Spin Transfer Torque (STT) promises to greatly reduce the power and die area and improve the writing selectivity. The excellent writing/reading, power, and area performance of STT-MRAM makes it one of the best nonvolatile memory candidates.



Fig(4).STT-MRAM based FPGA

circuits first benefit from the non volatility of MRAM to store the configurations both in LUTs and Interconnects and the high writing speed of MRAM cells may also have a strong impact on the chip architecture. Intermediate data normally stored in D-flip-flops can be stored in MRAM cells, and any block can then be safely powered off, which allows the MRAM-based FPGA hard to noise or power failure. In an SRAM-based FPGA, all SRAM cells may be initialized and kept with the configuration information during computing; besides, most of them are in “idle” state.

C.DISADVANTAGES IN EXISTING ALGORITHM

1.There may not be sufficient operational margin to ensure reliable resistance-to-voltage conversion.

2.Emerging memory technologies may suffer from relatively high defect density and/or write failure rate.

3.They may not be able to use conventional memory fault tolerance techniques to handle the defects and write failures.

D.ADVANTAGES OF PROPOSED ALGORITHM :

1.The main advantage is it considerably reduces the silicon area.

2.Speed performance improvement at relatively small DRAM refreshes the cost.

3.It incurs no negligible extra energy consumption.

VI.CONCLUSION

The fully centralized design style is a more viable option for this concept. In the fully centralized design approach, a single embedded MRAM block is used to persistently store the configuration data and initialize the distributed SRAM cells during power-up. Even assuming the use of error correction codes for memory defect tolerance, this design approach only results in an area

overhead of 7.9% and can maintain almost the same speed performance as conventional design practice. But our proposed new design to replace the SRAM cells with dynamic random-access memory (DRAM) cells to reduce the area and use embedded MRAM to refresh DRAM cells. We elaborate on the analysis of cost induced by periodic on-chip DRAM refresh. Replacing embedded Flash memory in the centralized design style, embedded nonvolatile memory could potentially make it more feasible to replace distributed SRAM cells with distributed DRAM cells.

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WEB RESOURCES

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[2]http://www.slideshare.net
[3]Lattice Non-volatile FPGA [online],Available: http://www.latticesemi.com/products/fpga/index/.cfm.