Comparative Analysis of 6T and 5T SRAM for Recovery Boosting Concept

P. Sivakumar [1], Jenyfal Sampson [2] , Vignesh Kanna. R [3], Vijay.P [4], YogeshWaraSiva.R [5]
[1] Professor, Email: siva@klu.ac.in, [2] Assistant Professor., Email: jenyfal@gmail.com,
[3], [4], [5] Student, B-Tech Electronics and Communication Engineering,
Email: vkannaece94@gmail.com, vijaysri.sri9@gmail.com, siva94@gmail.com
Electronics and Communication Engineering, Kalasalingam University.

***Abstract*— SRAM is a major source to store the data's for a long time. This device could consume more power depending on the design of the circuit. One of the major reasons for this power leakage is due to the two Bit Lines. This leakage should be reduced for better performance of the circuit and also in avoiding chip damage. The manufacturing by using two bit line circuit contains poor performance and high leakage. In this paper we are going to reduce the power, by designing the circuit by using single Bit Line. In single Bit Line SRAM, only one read Bit Line is being used and the voltage level at another Bit Line node is remains low. Single-BL reading is achieved by using a left access transistor and a left shared reading port. In addition, a new sense amplifier circuit without reference voltage is proposed for single-BL reading. When comparing 6T and 5T, 5T requires low power, so we are proposing single bit line using recovering boosting concept.**

***Keywords*— 5T, 6T, Adiabatic, Recovery Boosting, Bit-line Reduction.**

I.INTRODUCTION

Advances in technology have raised many new issues Today's extremely complex VLSI chips have been designed to reduce power and performance by stretching the limits of available technologies. Semiconductors have seen a revolution over a decade and the trend will continue in terms of area, speed and power. With continuous scaling of the devices to minimize feature size, power and performance have become the most important concerns. To meet the performance requirements, the amount of embedded SRAM in modem microprocessors and systems- on-chips (SOCs) has increased.[1] Thus designing SRAM cell that consumes low power is highly desirable. As the demand of portable devices increasing day by day with a strong battery backup and less power consumption became the most important consideration in today's world [2].

The Double Bit-line cell [Fig. 1] loses its reliability at low supplies due to degraded noise margins. So a large number of her cells have been proposed that increase the stability of the cell. The SRAM yield on these metrics can be rapidly estimated through stochastic simulation techniques such as response surface model or importance sampling. This paper suggests a technique to estimate the read stability and write ability of 6T cells from peripheral measurements of the physical SRAM cells without changing the array structure. An alternative measurable stability metrics for read and write is being surveyed and then modified to improve the correlation with the conventional stability definition. By simulation the estimation error sigma for read stability and write ability will be carried out. It has found its applications in the area of wireless sensor networks. [3][4].

II.EXISTING SYSTEM

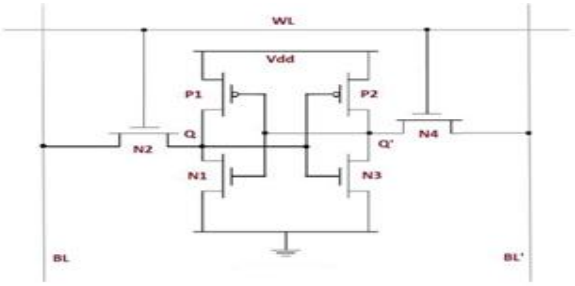
Bit line leakage is the major reason for power consumption. Single bit line based adiabatic technique. The read noise margin is low for two BL SRAM [5] and the Bit Line leakage does not giving the better performance of the circuit.

READ OPERATION : Precharge BL,BL' to High and Turn on WL .BL or BL' will be pulled down to LOW depending on Q,Q' .Eg: If Q=0,Q'=1, discharges through N2-N1-GND and BL' stays high ,But Q bumps up slightly. In order for Q to not flip N1 should be stronger than N2, ie N1>>N2

WRITE OPERATION: Drive Bl, BL' with necessary values. Turn on WL.Bit Lines overpower cell with new value Eg: Q=0, Q= and BL=1, Bl'=0.This forces Q' to low and Q'to high . To overpower feedback inverter loop, N2 should be stronger than P1, ie N2>>P1.

In proposed circuit we assume that 16 cells are connected to the BL. The BL is connected to the global bit line (GBL) via the write and read ports. They are activated by the write port switch signal (WPSW) and the read port switch signal (/RPSW). Only the read word line (RWL) goes high during reading, while both the RWL and the write word line (WWL) go high during writing. The proposed SRAM uses the read port to reduce the BL capacitance; that is, connecting only 16 memory cells to the BL dramatically reduces the BL capacitance. So, the BL is totally discharged to GND. This read port provides a large DNM. The increasing market of mobile devices and battery powered portable electronic systems is creating demands for chips that consume the smallest possible amount of power. Memories are the biggest culprit for the power dissipation in any digital system

because SRAM [6] consist of almost 60% of Very Large Scale Integrated (VLSI) circuits and No digital system gets complete without memories. The speed and power consumption of SRAMs are important issue [7] that has lead to multiple designs with the purpose of minimizing the power. A stepwise waveform from a tank capacitor is suitable because of its stability. This charging operation is adiabatic in both the thermodynamic and mechanical senses. The tank capacitor circuit does not have to be on the same chip as the SRAM; the stepwise signal just has to be input into the SRAM chip. The tank capacitor circuit is closer to a digital than an analog circuit because it only outputs the voltage of the tank capacitor.



ig. 1. Two BLs are used.

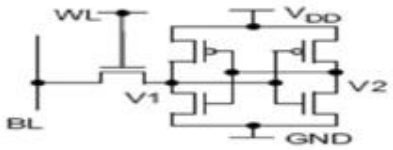


Fig. 2. Single BL is used, for reading.

READ OPERATION: Considering the case of reading Q=0; before reading a value from the storage nodes, the bit line BL is precharged to VDD. The read word line RL is then VDD is asserted. The storage node Q' that stores a 1 is statically connected to the gate of MRA (Read Access Transistor) and will drain the charges on the bit line through MRD to GND as the RL is 1, which means that the bit line has just read a 0. On the contrary, when Q=1, Q' will be 0 and MRA will be in cut off and the bit line BL would not be able to discharge through MRD to GND, and it would read a 1.

In this system the negative bias temperature instability is a reliability problem in microprocessors. The earlier techniques only aim to balance the degradation of the two PMOS devices by attempting to keep their inputs at a logic '0' bit. Always one of the devices is in NBTI.

III.PROPOSED SYSTEM

The proposed 5T SRAM cell [Fig. 2] is designed by considering the standard 5T SRAM cell. In this design the bit-line and bit-line bar of the conventional 5T SRAM cell is replaced by single bit-line for both read and write operation. The proposed design has increased the read stability and SNM, without affecting the chip Size or leakage Power Consumption of a Standard 5 Transistor SRAM cell. The proposed 5 Transistor new SRAM Cell is created by adding two more transistors MRA (Read Access Transistor) and MRD (Read Driver Transistor) which shall work independently during read operation and won't affect the Cell SNM in any way [9].

Memories are an integral part of most of the digital devices and hence reducing power consumption of memories as well as area reduction is very important as of today to improve system performance, efficiency and reliability. Most of the embedded and portable devices use SRAM cells because of their ease of use as well as low, a transistor that means that it is not turned on when there is a voltage potential. In mechanics, on the other hand, an adiabatic change is a slow deformation of a state in which a certain parameter changes very slowly. In our circuit, that parameter is the WL voltage .A five-transistor SRAM cell (5T SRAM cell) is conventionally used as the memory cell. 9 Therefore, conventional SRAM cells that use the 5T RAM cell have difficulty in meeting the growing demand large memory capacity in mobile applications.

WRITE OPERATION: The word-line WL is charged to VDD as in 5T Standard SRAM. Since NMOS is a stronger driver than PMOS, no problem is incurred while writing a 0 into the cell. The absence of the pull down in the NMOS for memory node Q allows cell easily in writing 1. Writing a 1 is done by pre-charging bit-line BL to VDD. While writing 0, the bit-line BL is discharged and then word-line WL is charged to VDD as in 5T Standard SRAM.

Limiting the power consumption with new architectures are the design requirements in recent integrated circuits. In the case of SRAM, one seemingly counter intuitive approach is to utilize only a single bit-line without jeopardizing read stability, which leads to the development of a Single Ended 5T SRAM. The proposed new SRAM cell gives a significant power reduction by reducing the switching voltage on bit lines. The power consumption is reduced by reducing the switching voltage between the read and write operation

IV.RESULT AND ANALYSIS

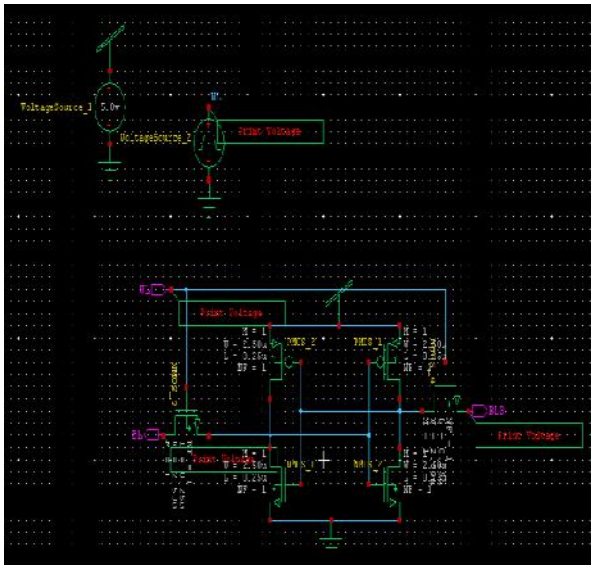


Fig.4. Circuit of 6T SRAM Cell3

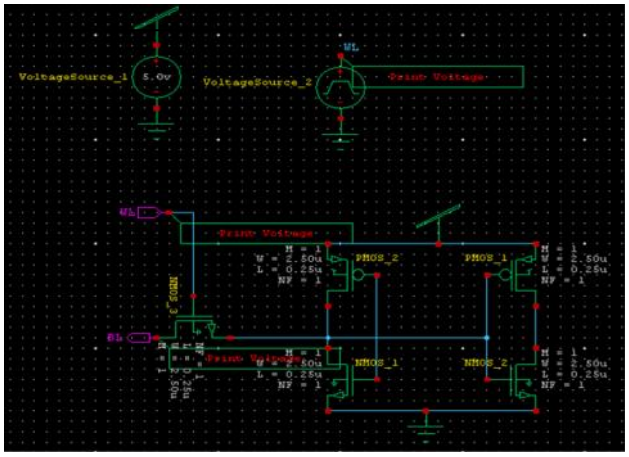


Fig.4.1.Circuit of 5T SRAM cell

VI.CONCLUSION

In this paper, we have reduced the power based on recovery boosting concept, when compared to 6T and 5T. This is much suitable for embedded memory application as it reduces leakage and power .This work can be enhanced using CMOS technique that is suitable for SRAM.

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TABLE I

COMPARISION of DOUBLE BIT-LINE and SINGLE BIT-LINE

COMPARISON

FACTORS	DOUBLE BIT-LINE	SINGLE BIT-LINE
1.Average power consumed	7.166581e-003 watts	1.244444e-003 watts
2. Max power	9.025e-007 watts	4.39777e-009 watts
3. Min power	8.04931e-007 watts	8.025e-007 watts
Transistor count	6T	5T
Computational Time	1.67 seconds	1.60 seconds

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