Design and Characterization of Standard Cell Inverter1X2 for DSM Process

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***Abstract*-- Standard cell is a pre implemented logic, optimized and kept in a part of the library. Standard cell design is a challenging task faced by VLSI chip designers. Traditional methods of standard cell design automation rely on a schematic representation supplied by a design engineer. These are designed in the full-custom flow and used in the semi-custom flow (ASIC). This paper presents the backend designing of a standard cell** Inverter1X2 **for DSM process (90nm technology) and characterizing them for different simulation corners.**

I. INTRODUCTION

VLSI is a field which involves packing more and more logic devices into smaller and smaller areas. Because of VLSI it has become possible to design the complex digital circuits in a simple way, so that the space, power inputs and the cost can be considerably reduced. The VLSI industry adopts a particular design methodology in order to achieve the control over the above said parameters[1-3].

Standard cells are widely employed in VLSI circuits such as computer, car, digital camera, the cell-phones, including the chips controlling nuclear plants, aircrafts, satellites, space vehicles etc[4].

The silicon CMOS technology has become the dominant fabrication process for relatively high performance and cost effective VLSI circuits[5]. In simple terms, the fabrication refers to the sequence of steps that we use to take a bare "wafer" of silicon to the finished form of an electronic integrated circuit[5]. CMOS circuits are designed by creating nFETs and pFETs in silicon and then wiring them together using interconnect lines formed on the conducting layers[5].

A. Design flows

i. Full Custom Flow

The full custom flow is also called as analog flow which is used to design analog devices such as amplifiers, oscillators etc. This flow involves the usage of only hundreds to thousands of transistors which can be handled manually. The steps involved in this flow are as follows,

Specification : The parameters specified in this step are length and width of the transistor, voltages and temperatures to be operated, setup and hold time, and number of inputs and outputs etc.

Schematic/Circuit : Using the above specifications the required circuit is designed which is easy to analyze as shown in Fig 1.

Simulation : This is done to check the functionality of the circuit.

Layout : The layout is designed according to the details given by the foundary document, for the required schematic and is fabricated on the silicon wafer. After designing the layout DRC, LVS, PEX and COMPATIBILITY checks are performed.

Tapeout : After all the above steps the design is sent for fabrication. Some of the fabs are TSMC, UMC, IBM , INTEL etc[6].

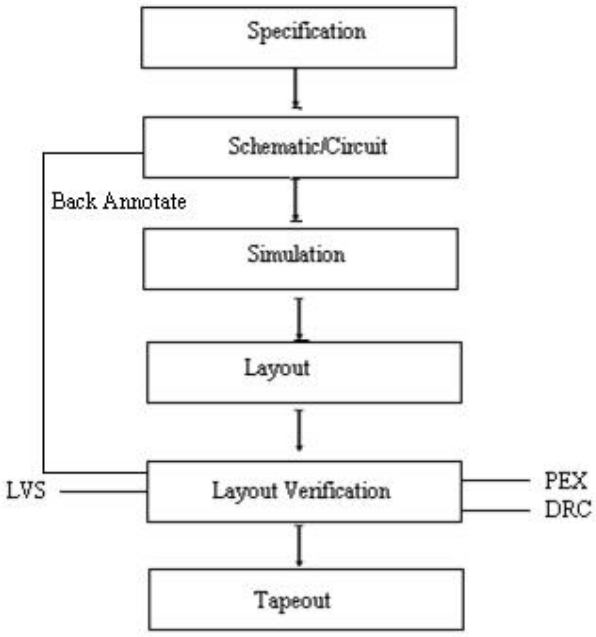

Fig.1. Full custom flow

ii. Semi custom flow

Fig 2 shows the semi custom flow. This flow is extensively used in ASICs or Application Specific Integrated Circuits, Progress in the fabrication of IC's has enabled us to create fast and powerful circuits in smaller and smaller devices. This also means that we can pack a lot more of functionality into the same area. The biggest application of thisability is found in the design of ASIC's. These are IC's that are created for specific purposes - each device is created to do a particular job, and do it well. The most common application area for this

is DSP - signal filters, image compression, etc. To go to extremes, consider the fact that the digital wristwatch normally consists of a single IC doing all the time-keeping jobs as well as extra features like games, calendar.

Specification : The parameters specified in this step are length and width of the transistor, voltages and temperatures to be operated, setup and hold time, and number of inputs and outputs etc.

Architecture : Here the circuit flows are represented in blocks.

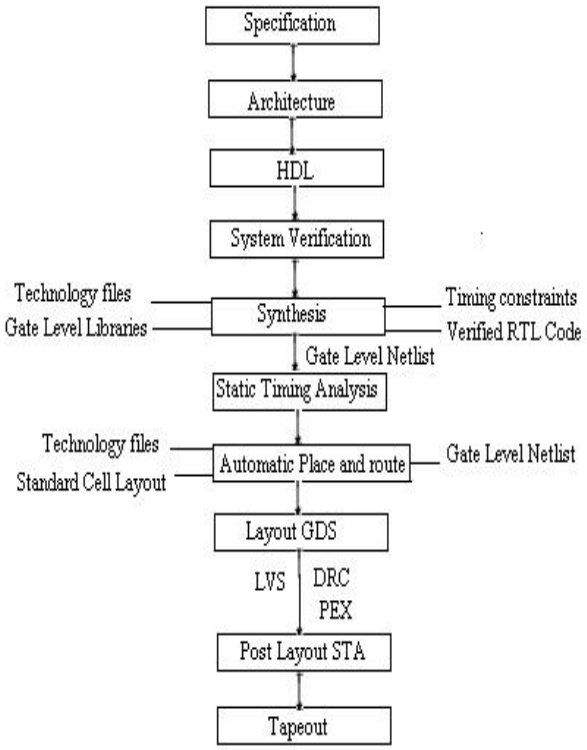

Fig2: Semi custom flow

HDL : This process is analogous to writing a computer program in a high-level language. This is usually called the RTL (Register Transfer Level) design. Designers of digital ASICs use a hardware description language (HDL), such as Verilog or VHDL, to describe the functionality of ASICs.

System Verification : Here an artificial environment in which the chip has to operate is created.

Synthesis : The inputs for the synthesis are verified RTL code , gate level libraries and technology files. The output of the synthesis is the gate level netlist.

Static Timing Analysis (STA) : This performs Timing Checks which examines whether the chip is working in the given frequency range. This also makes sure that there are no setup and hold time violations. This fixes only setup time violations.

Automatic Place and Route : Gate level netlist , Standard cell Layout and Technology files are the inputs for APR. This consists of Floorplannig , Placement of cells , Clock Tree Synthesis and Routing.

Layout GDS : The layout is designed according to the details given by the foundry document. After designing the layout the formal verification is done for DRC, LVS, PEX and COMPATIBILITY checks.

Post layout STA : Clock Tree Synthesis is mainly generated in this stage. All the hold violations are corrected here.

Tapeout : After all the above steps the design is sent for fabrication[7].

B. Related work on standard cells

Standard cells are logic units used in ASIC design flow. They are pre-designed cells by considering three factors: area, speed and power dissipation. Behavior of these cells with respect to varying load, supply voltage, spice models and temperature is well understood and captured over a wide range of operating conditions such that these cells can be re-used in the ASIC flow. There by bringing down overall design cycle time. The project aims at designing and characterizing the standard cells for standard DSM process. In DSM (Deep Sub Micron) process the designs are achieved in areas deep into micron ranges of the “Silicon Real Estate”. Here the supply voltage is scaled down to prevent reliability hazards such as oxide breakdown and also to reduce energy per operation of digital circuits. Examples for standard cells are NOT, AND, NAND, NOR, LATCH, FLIPFLOP, Half Adder etc. Behavior of these cells with respect to varying load, supply voltage, spice models and temperature is well understood and captured over a wide range of operating conditions such that these cells can be re-used in the ASIC flow. There by bringing down overall design cycle time[8, 9].

C. Contribution:

This paper involves the designing and characterizing of Inverter1X2 for a 90nm technology. Here for each cell a pre layout simulation and a post layout simulation are performed. Emphasis is placed on presenting the details of translating a system specification to a small piece of silicon. Within the bounds of MOS technology, the possible circuit realizations may be based on nMOS, pMOS, CMOS and BICMOS.

The pre layout simulation involves Schematic Entry, extracting the net list from it and finally running of test bench for various simulation corners. In case of post layout simulation at first a layout for the required schematic is drawn

using various MOS layers such as polysilicon, metal, diffusion layers etc. Using Fingers and Folding concept it is possible to reduce the area occupied by the standard cell considerably. After this a series of checks are performed to fix the errors if there are any. The checks are DRC, LVS, Compatibility and finally the PEX. The Design Rule Checking (DRC) determines whether the physical layout of a particular chip layout satisfies a series of recommended parameters called Design Rules. Design rule checking is a major step during Physical verification on the design. The Layout versus Schematic (LVS), this process confirms that the layout has the same structure as the associated schematic; this is typically the final step in the layout process. The LVS tool takes as an input a schematic netlist and the extracted netlist from a layout and compares them. Nodes, ports, and device sizing are all compared. If they are the same, LVS passes and the designer can continue. The Compatibility checks are performed to see whether the I/O pins are placed in the correct position or not. Parasitic Extraction (PEX) is extracting the measure of Resistance and Capacitance involved in the design which contributes for the circuit delay. The Foundary Document provides with information into the various DSM technology processes, layer descriptions, layer derivations, Mask sets, Design Rules constraints, metal layer parameters and their associated sheet resistances. After doing all these steps it is necessary to see the waveforms of the required circuitry to check the functionality. In current ASIC designs, cell-base design methodologies are widely used. High-quality cell libraries are crucial for designing high-performance circuits. Recently cell-based design with various driving strength cells is discussed and it is found that a rich library in driving strength improves circuit performance close to transistor-level optimized circuits. Cell libraries including a plenty of driving strength variation for 90nm technologies has been developed. Library whose cell heights and widths are different is provided. One is for high-speed and various PVT (process, voltage & temperature) corners. The functionalities of their libraries are verified by the measurement of the fabricated chips.

II. STANDARD CELL ARCHITECTURE

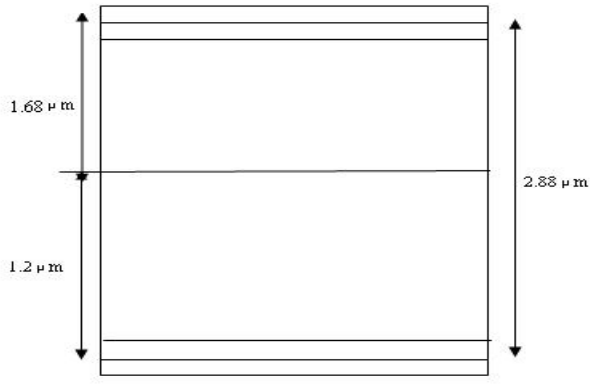

Fig 3. Standard cell structure, N-well ht=1.68µm, total std cell ht = 1.68µm+1.2µm=2.88µm.

The height of a standard cell is fixed. In our case it is 2.88µm. The length of NWell covered pr boundary should be 1.68µm. The Standard cell chosen is nand with different inputs and drive strengths. The organization of each library in logical function and driving strength is the same. The driving strength range is from x0.5 to x32 and it advances the flexibility to various load and conditions. Small driving cells (x0.5) are so effective to reduce power dissipation. Small increase step in driving strength enables fine tuning in delay and power optimization[4].

Inverter1X2: INVERTER Basics

NAND Gate is one of the two universal gates since combinations of it can be used to accomplish any of the basic operations and thus can produce an INVERTER, basic OR , and an AND gate. The non-inverting gates do not have this versatility since they can't produce an invert.

TABLE 1
TRUTH TABLE OF NAND

A	C
0	1
1	0

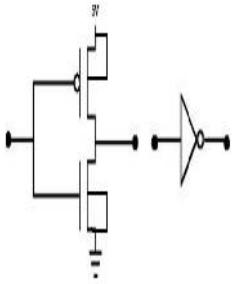

Fig. 5. INVERTER1X2

- P/N Ratio=µ=2.29
- N MOS = l/w*2 = 0.1/0.49*2 =0.1/0.98
- P MOS = l/w*µ*2 = 0.1/0.49*2.29*2 = 0.1/2.24

If both of the A and B inputs are high, then both the NMOS transistors (bottom half of the diagram) will conduct, neither of the PMOS transistors (top half) will conduct, and a conductive path will be established between the output and V_{ss} (ground), bringing the output low. If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and V_{dd} (voltage source), bringing the output high.

III.STANDARD CELL LIBRARY DEVELOPMENT FLOW

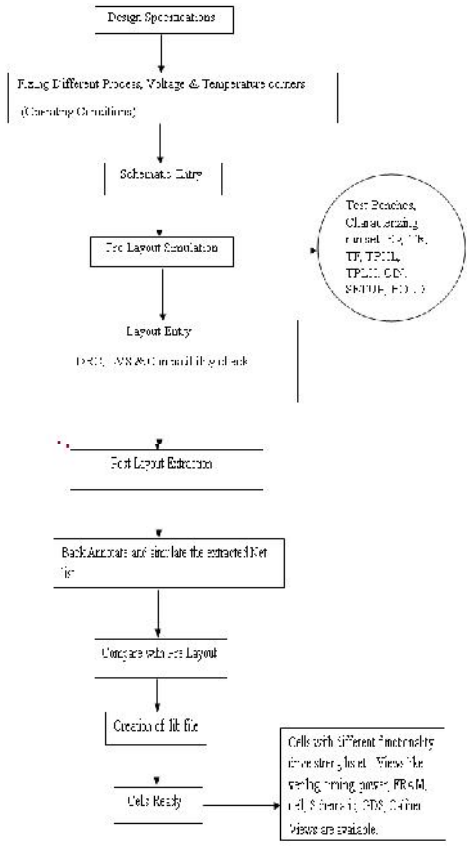

Fig. 6. Standard cell library development flow

IV. SCHEMATIC AND LAYOUT VIEWS

Source and Drain sharing method between neighbour inverters are utilized in order to decrease the area covered by circuit. However, complicates the routing of interconnections. Only Metal1 is used for routing though it is a 9 metal process to make metal 2-9 available to the router. Layout is a physical representation as it would be manufactured. The physical layout perspective is a "bird's eye view" of a stack of layers. The circuit is constructed on a p-type substrate. The polysilicon, diffusion, and n-well are referred to as "base layers" and are actually inserted into trenches of the p-type substrate. The contacts penetrate an insulating layer between the base layers and the first layer of metal (metal1) making a connection. The inputs are given in polysilicon (illustrated in green color). The CMOS transistors (devices) are formed by the intersection of the polysilicon and diffusion; N diffusion for the N device & P diffusion for the P device (illustrated in red color with corresponding implats coloring blue and white respectively respectively). The output is connected together in metal (illustrated in blue coloring). Connections between metal and polysilicon or diffusion are made through contacts (illustrated as greensquares). The physical layout should match the logic circuit and the schematic.

- ✓ Assumed contacted diffusion on every s / d.
- ✓ Good layout minimizes diffusion area
- ✓ Ex: NAND3 layout shares one diffusion contact
- – Reduces output capacitance by 2C
- – Merged uncontacted diffusion might help too

The N device is manufactured on a P-type substrate while the P device is manufactured in an N-type well (n-well). A P-type substrate "tap" is connected to V_{SS} and an N-type n-well tap is connected to V_{DD} to prevent latchup.

B.inverter1X2:INVERTER schematic and layout

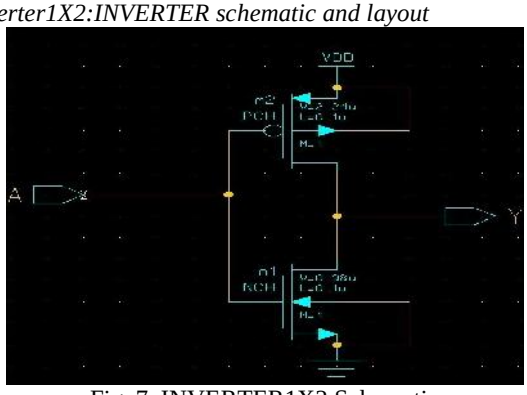

Fig. 7. INVERTER1X2 Schematic

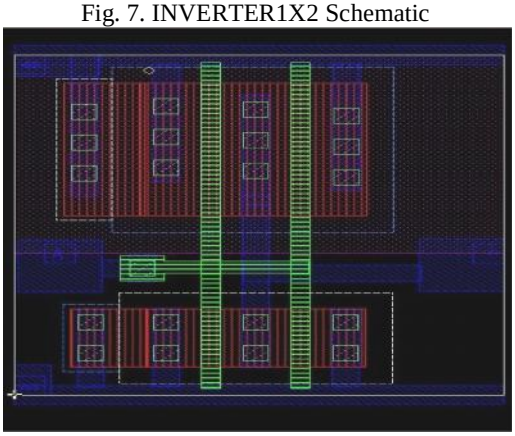

Fig. 8 INVERTER layout

V. PRELAYOUT SIMULATIONS

. The following subsections detail the test setup for characterization.

For Pre-Layout

1. ICstudio is opened in the REDHAT Linux environment.
2. In icstudio all the required standard libraries are added.
3. Using the tools from the added standard libraries such as generic_lib, source_lib, device_lib etc, the schematic of the NAND is drawn in schematic editor.
4. Check and Save is performed on the schematic and the netlist is dumped out.
5. Simulation is done on the dumped netlist and generated testbench for different slew rates, output load and for various characterization and simulation corners such as SSLVHT, SSHVLT, SFLVHT, SFHVLT, FSLVHT, FSHVLT, FFLVHT, and FFHVLT.
6. TR, TF, TPHL, and TPLH and eldo logs are obtained.

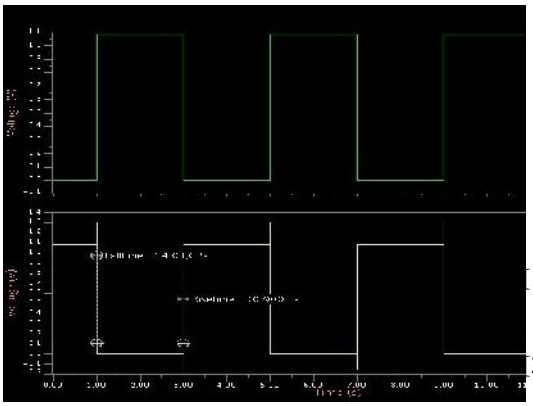

Fig. 9. INVERTER Functionality with TR and TF

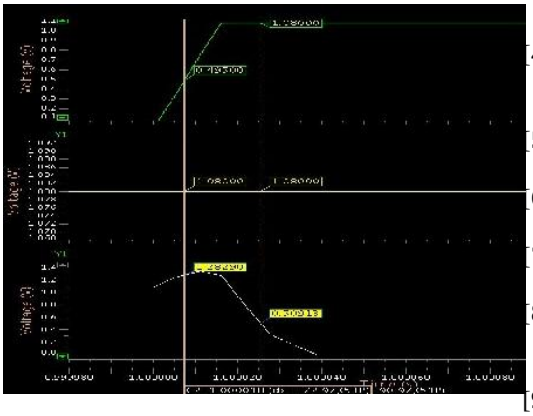

Fig. 10. Propagation delay low to high.

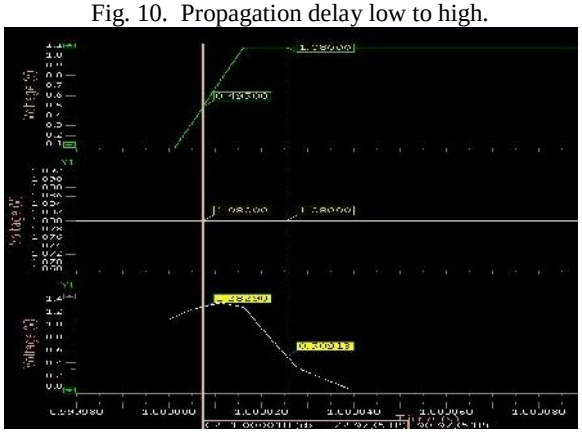

Fig. 11. Propagation delay high to low.

VI. POST LAYOUT SIMULATIONS

1. The NAND layout is designed in the polygon editor using different layers provided by the tool and according to the rules provided in the Foundry Document.
2. Layout is designed using Fingers and Folding concept in order to make the cell size compact.
3. LVS, DRC, PEX and Connectivity checks are performed on the designed layout.

VII. CONCLUSION

The higher frequency of operation with control over area and power has been designed. Semi-custom application specific integrated circuit design methodology is the alternate to a FPGA implementation flow to achieve aggressive area, power and timing budgets. Thus a working standard cell library compatible with other technologies has been designed.

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