Approach to design a Low Power Consuming Double-Tail Comparator

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Abstract:

Comparators are the most analyzing unit in the analog to digital converters. In such situation the high speed and the low power consumption based comparators are used. Hence designing of comparators are more challenging when the supply voltage is smaller. The existing low power consuming dynamic comparator designed to be used in ADC's is considered. With reference to that design a new low power consuming double- tail comparator is designed by using clock gating technique to reduce the power leakage.

***Index Terms*- Double tail comparator, high-speed analog-to-digital converter,**
low-power analog design.

I.Introduction

A comparator is the simplest circuit that moves signals between the analog and digital worlds. It allows the trigger to drive the output either high or low as needed in the circuit which can be inverting or non-inverting. Essentially a comparator circuit is a 1-bit analog to digital converter, with a selectable conversion point, which makes the comparator act as a switch triggered by a signal on its input [1].As comparators plays a significant role in analog to digital converters, it is very important that they consume low power and works at high speed. To reduce the power consumption by the comparator the total amount of power dissipation in the circuit must be scaled.

An increase in power dissipation at constant performance occurs as the result of lowering the analog supply voltage. This becomes drastic as the supply voltage approaches the threshold voltage plus a few hundred millivolts [4].Power dissipation is quickly becoming a bottleneck for future technologies. Many circuit techniques have been proposed to reduce these dissipations in VLSI circuit design.Clock gating is a well-known technique to reduce power dissipation in the circuits.As individual circuit usage varies within and across applications not all the circuits are used all the time,giving rise to power reduction opportunity.The major component of microprocessor power is clock power because it is fed to most of the circuit blocks in the processor, and it switches every cycle.This technique is used in the proposed low power consuming double tail comparator to reduce power dissipation.

Effective clock gating ,however, requires a method that determines which circuits are gated, when it is gated and for how long. The either result in frequent toggling of the clock-gated circuit is performed using clock gating scheme between the enabled and disabled states ,or applied to such small blocks that the clock-gating control circuitry is almost as large as the blocks themselves, result of large overhead. This may result in higher power dissipation than those without clock gating.While the concept of circuit-level clock gating is widely known, good architectural methodologies for effective clock gating are currently being developed.

The existing low power consuming dynamic comparator was designed by modifying the circuit of the conventional double tail comparator for low power and fast operations even in small supply voltages.

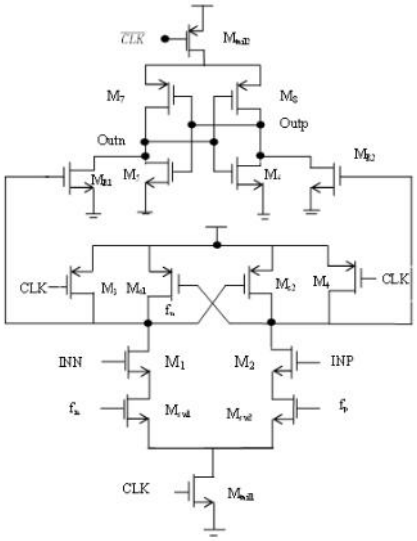

Fig 1. Schematic diagram of Low Power Dynamic Comparator

Based on the existing circuit, in the proposed low power consuming double tail comparator few transistors are added to the chip area. This modification also results in

considerable power savings when compared to the conventional double-tail comparator.

II. Low power consuming Dynamic Comparator

High-speed ADCs uses Dynamic comparators widely due to its low power consumption and fast speed [2].The operation of this comparator is as follows.The schematic diagram of the circuit is shown in the Fig1 and the Fig2 is the waveform of the simulated circuit. During reset phase, CLK=0, Mtail1 and Mtail2 are OFF, avoiding static power, the control transistors are in cut off stage when M3 and M4 pulls both fn and fp nodes to VDD.The intermediate transistors MR1 and MR2 resets both latch outputs to ground.

During comparison phase ,CLK=VDD, transistors Mtail1 and Mtail2 are On, M3 and M4 turns OFF. The static power consumption is avoided by using two NMOS (Msw1 and Msw2)

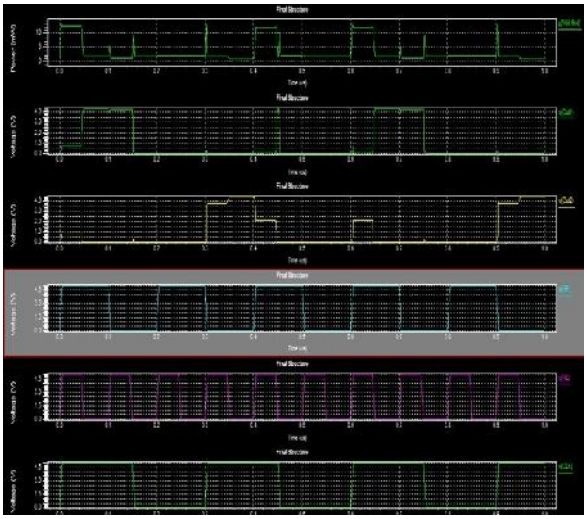

Fig 2. Waveform of low power consuming dynamic comparator

switches. Proposed comparator enhances the speed of the double tail comparator by affecting two factors such as increases the initial output voltage difference at the beginning of regeneration (t=t0); and it enhances the effective trans conductance.

Performance in terms of speed and yield can be achieved for an input dc level of 70% of the supply voltage [3].The INN, INP are the input voltage and fn and fp are reference voltage.This structure has the merit of high input impedance and good robustness against noise.In the above structure the upper part of the comparator forms the one tail and the lower part forms the other tail.The second tail is modified inorder to design the proposed circuit.The waveform of the clock output rises and falls.It rises when there is supply of voltage and falls when there is no supply.

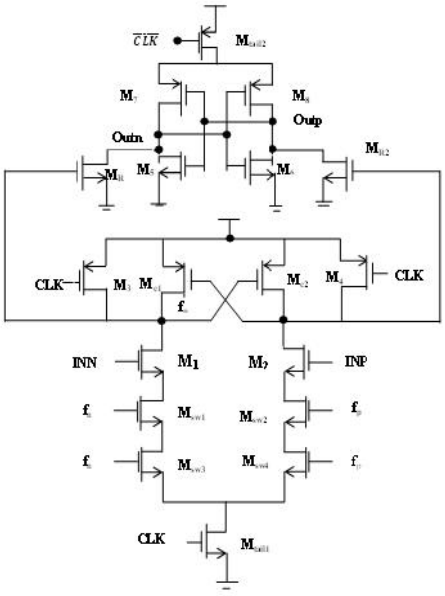

Fig 3. Schematic diagram of Low Power Consuming Double-Tail Comparator

III. Proposed Low Power Consuming Double-Tail Comparator

The schematic diagram of the proposed circuit is shown in the Fig3.The simulated circuit waveform is Fig4.Operation of modification in both reset and comparison phase is similar in proposed comparator .At the beginning of the decision making phase, nodes fn and fp have been precharged to VDD.The node fn and fp starts to drop with different discharging rates in the reset phase and the switches are closed.

Control transistors will act in a way to increase their voltage difference as soon as comparator detects that one of the fn/fp nodes is discharging faster. Ultimately switching in the charging path of fp will be opened but to allow the complete discharge of fn node the other switch connected to fn will be closed if fp is pulling up to VDD and fn should be discharges completely . The operation of the latch is emulated by the operation of the control transistors with the switches.

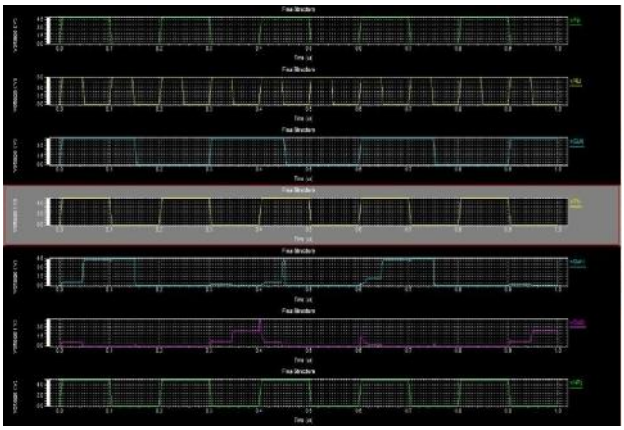

Fig 4.Waveform of low power consuming double- tail comparator

The transistors size can be determined by the time it takes that one of the control transistors turns on must be smaller than t0(regeneration time).It can be achieved by designing first and second stage of tail currents. Low threshold pMOS devices can be used as control transistors leading to faster turn on in the fabrication technology. Another consideration is effect of mismatch between the controlling transistors of the comparator. Mismatch is a spatial noise spread. Mismatch effect is reduced in this modification. The large voltage variations in the internal nodes are coupled to the input disturbing the input voltage called kick back noise. Most efficient comparators generate this type of noise. The minimum kickback noise is in the double tail comparator.The first stage with the transistors M1–M4 and M9 is the amplification stage.More practically, by using the pre-amplifier preceding the regenerative output latch stage,the input-referred latch offset voltage can be reduced.

Table 1

Performance Comparison

Comparator Structure	Low Power Dynamic Comparator	Low Power Double-Tail Comparator
Technology	180nm	90nm
Supply Voltage	0.8v	0.8v
Power	0.3742403 watt	0.3603853watt
No. of Transistors Used	16	18

To overcome the latch offset voltage it can amplify a small input voltage difference to a large enough voltage. The second stage is comprised of the transistors M5– M8 and M10 regenerative(evaluation) phase that forms the regenerative stage. The tail transistor M9 turns ON and M10 turns OFF when the clock (CLK) is low (amplification phase).

Here only amplification stage works when CLK is LOW. The amplification stage is designed to effectively reduce the charging time to produce its output close to VDD. In this stage fp-fn is amplified and fed to regenerative stage. The transistors M10 turns ON and M9 turns OFF when the clock (CLK) is high (regeneration phase). Only regenerative stage works here. Over the double tail latched comparator there is a reduction of the delay time in the pre-amplifier based clocked comparator. But the pre-amplifier based clocked comparator consumes static power using an amplification stage during the amplification period and hence the energy consumption in the pre-amplifier based clocked comparator becomes higher than the double tail latched comparator.

However,it suffers not only from large power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance due to the continuous technology scaling.

There is a reduction of the power dissipation in the double tail latch comparator over the pre-amplifier based clocked comparator.

IV.Result Analysis

The performance comparison is given in the Table1. It is analysed that the power consumption of the proposed circuit is decreased when compared to the existing circuit.

V. Conclusion

The low power consuming double-tail comparator is designed in which clock gating technique is used to reduce the power consumption.Few transistors are added to the circuit due to its high impedance characteristics.These comparators are widely used in the analog to digital converters.The main objective of designing this comparator is to make ADC's to work with high speed consuming low power.

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