AN EFFICIENT 3D DETAILED ROUTER APPLYING REGULAR ROUTING PATTERNS

S.R.Subathra[1], S.B.Subbulakshmi[2], R.Sujitha[3],
B.Tech Scholar, ECE Department,
Kalasalingam University
subathrasr6@gmail.com,
subbulakshmisb94@gmail.com,
lithikasujisri@gmail.com

K.Pandiaraj[4] M.E,
Assistant Professor II,
ECE Department,
Kalasalingam University
pandiaraj@klu.ac.in

Dr. P. Sivakumar[5]
Assistant Professor,
ECE Department,
Kalasalingam University
siva@klu.ac.in

ABSTRACT:
VLSI generally consists of partitioning, placing and routing. Routing is interconnecting local nets with a set of wires. It could be done only in dead space or white space and cannot be routed if there is a blockage. It is of two types namely Global Routing and Detailed Routing. With Global Routing as base Detailed Routing is to be done. Detailed router is made to follow regular routing patterns and a regular route is applied for better design and rule satisfactory in order to avoid jogs and detours. Here 2D Detailed routing tracks, spacing based design rules are to be discussed. Routing of local nets are to be done before global segment assignment using bottom up layer by layer and panel by panel framework. To reduce congestion Panel Merging and Maze Routing techniques are to be used. With the help of benchmark circuits label position and congestion prevailing among local nets are to be determined. Reducing the white or dead space is to be done by Panel Merging technique.

INTRODUCTION:

A router needs to be an efficient one. Efficiency deals with time, delay, speed and power. If these are efficient a system is said to be efficient. But this is not practically possible as it consists of a lot of constraints as jogs, detours and blockages. In order to make an efficient router VSRT, bottom up layer by layer, Panel Merging and MWIS techniques are to be used. While routing from a source to a destination it could be routed only through white space or dead space not through obstacles. To make a route as an efficient one shortest path has to be chosen along with a regular routing pattern making the routing process easier. Regular Routing also introduces less wire length improvising time, signal integrity and power consumption. Routing of each net could be done using maze routing along with rip-up and re-route technique. Regular route performances are to be analyzed from ISPD98 benchmarks.

PROBLEM FORMULATION:

Inputs are based on underlying spacing based rules, 2D global routing solution. If a 2D global routing solution is to perform automatically layer assignment and detailed routing is solved. The main objective is to connect and route as many nets as possible. In general global routing generates 3D solution where it is more restrictive with a lot of constraints. It does not provide relevant information to perform layer assignment and local nets are also not captured. Where detailed routing captures both local nets and global segments. It should be noted that each segment has to be assigned to a track to make it less restrictive, assignment to more than one track also occurs but it is not preferable.

ALGORITHM FLOW:

The process starts with extracting all global segments. And routing of local nets has to be done before global segment assignment or else it leads to blockages. A number of layers constitutes to a single panel. And routing has to be done from bottom layer, the last layers of the upper panel and the upper layers of the bottom panel remains unrouted. Maze routing techniques can be implied for those unrouted portion supported with rip-up and re-route technique. It is very effective in finding the label position of local net with the help of benchmark circuit and it is used to reduce the white space prevailing. If panels are merged, then routing becomes easier and regular routing patterns could be used without any constraints.

Then each layer is assigned with a certain weight and based on the priority routing is done. If it is an unrouted top layer Panel Merging and Maze Routing is done.

ALTERNATIVE FLOWS AND DISCUSSION:

Local nets could be routed by using vertical spine routing topology also. This helps to find out the interconnection properties to route mainly the local nets. It has its structure with x co-ordinate which is the median of all pins where each pin is connected to a central spine and based on weight of each pins routing is performed and leads to complexity of time. It routes as many nets as possible also constitutes in wire length minimization.

Always local nets has to be assigned before global segment assignment. This could be done by MWIS and solved by fast and effective heuristic optimization methods.

ROUTING CONSIDERATIONS:

NUMBER OF TERMINALS:

Majority of nets are two terminal ones and for some nets like clock and power, number of terminals can be large. Always each multi terminal net can be decomposed into several two terminal nets.

NET WIDTH:

Power and ground nets has greater width and signal nets has less width.

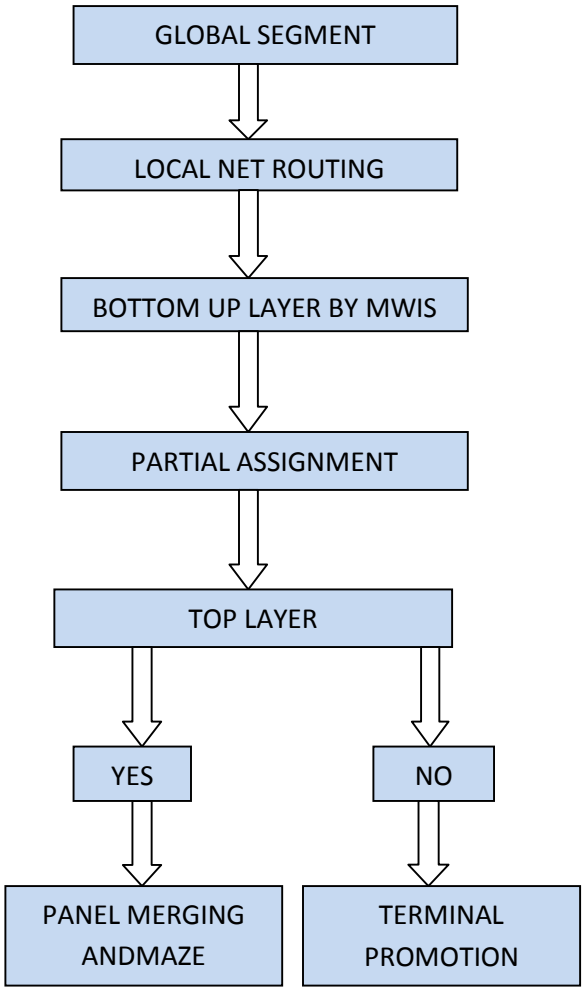


Fig 1. ALGORITHM FLOW

VIA RESTRICTIONS:

It is of two types namely regular which could be done only between two layers and stacked which could be done through more than two layers.

BOUNDARY TYPE:

It is of two types namely regular and irregular. It is also based on the net types and the number of layers.

UNASSIGNED SEGMENTS:

The probability of unassigned segments mainly occurs at top layers. And to improve the routability Panel Merging and Maze Routing is applied. Congestion is also prevented being more flexible. In Panel Merging technique one panel is merged with the neighboring panel and can be adjusted based on hardness level and runtime. It is more effective for the segment nearer to the panel boundary. At first, routing has to be done from lower layers and for unrouted portions line probing maze routing technique could be applied.

RESULTS AND DISCUSSIONS:

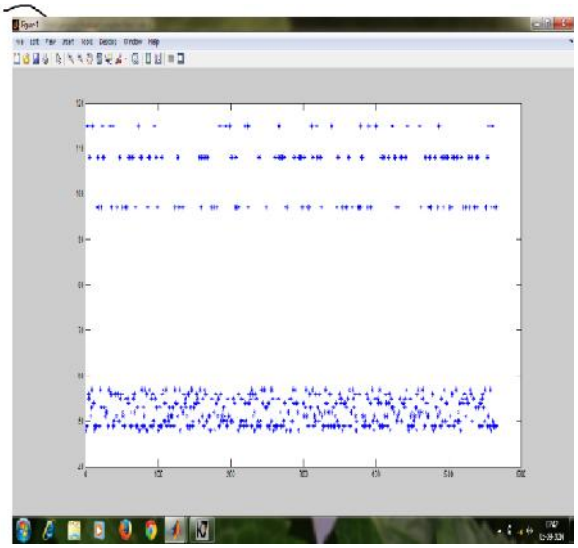
Experiments were performed based on the ISPD98benchmark results.

RESULTS OF REGULAR ROUTE FOR ISPD98:

This benchmark circuit consists of .net, .are, .netD file format. Each format consists of 22,500 modules, nets and pins. We worked to split those modules and read those using C and Matlab to convert those modules into array format to find the pin connections. All those connections were made as a grid graph pointing o of a label. And layers could be analyzed along with label position. But those local nets position in terms

We worked to merge all those layers reducng the white space to make routability effective. Congestion also could be controlled if a proper layer assignment is done.

OUTPUT:



CONCLUSION:

We have performed on the unassigned portions finding the local nets positions on a grid graph with ISPD98 results. Thereby decreasing the white space, congestion, local nets,

and wire length also. Our upcoming works will be to find the critical path, time, phase, delay and to merge out panels.

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