FPGA BASED PROTOTYPE FINGER VEIN RECOGNITION SYSTEM

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ABSTRACT-Finger vein recognition is a biometric authentication that uses pattern-recognition techniques based on images of human finger vein patterns beneath the skin's surface. The Vein ID is a biometric authentication system that matched with the vein pattern of individual's finger to obtain data. The technology is currently in use or development for a wide variety of applications, including credit and debit card, vehicle security, attendance, computer and network authentication, end point security and ATM etc. The simple, convenient, and high security authentication systems for protecting private information's stored in any kind of database devices has increased with the development of consumer electronics. The personal database's can be secured in any kind of biometrics which uses human physiological or behavioural features for personal identification. This project shows that Real Time Embedded Finger Vein Recognition System. The system is designing on a novel finger vein recognition algorithm which is implemented through DSP platform and Spartan 3AN.

INTRODUCTION

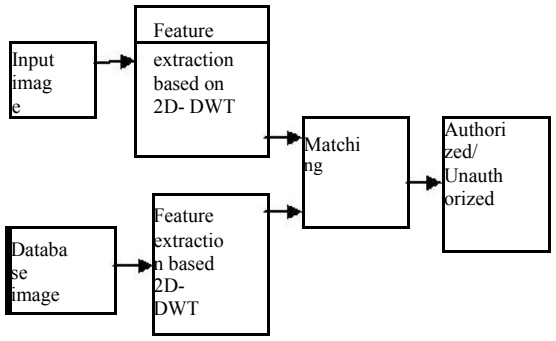
Private information is traditionally provided by using any passwords or key, which are easy to implement but it is to the risk of exposure and forgotten. Biometrics, uses human physiological or action for personal identification or finding, has preventing more attracted and more attention and is becoming one of the most popular and promising alternatives to the traditional password or PIN based authentication techniques [1]. Some consumer electronic appliances can be secured by biometrics ˙The list is developed and implemented, including the face, iris, retina , palm print , fingerprint, audio voice,signature and gait. This great and increasing variety of biometrics, no biometric has been developed perfectly. For example, fingerprints and palm prints are usually frayed having more line; voice, signatures, hand shapes and iris images are easily changed; face recognition can be made difficult by occlusions or face-lifts .such as fingerprints and iris and face recognition, are susceptible to spoofing attacks. The great challenge to biometrics is thus to improve recognition performance in terms of both accuracy and efficiency and be maximally resistant to deceptive practices yet at the same time, a highly

complex, hopefully challenge to those who wish to defeat them. Especially for consumer electronics applications, biometrics security systems need to be cost-efficient and easy to implement

˙The vein is a promising biometric pattern for personal identification in terms of its security and convenience ˙When compared with other traits, the vein has the following advantages: The finger vein is hidden inside the finger and it is invisible to human eyes, so it is difficult to steal. The non-invasive and contactless capture of finger-veins ensures both convenience for the user, and is it acceptable. The vein pattern can be taken from alive body. Therefore, it is a natural and convincing proof that the subject whose finger-vein is successfully captured is based on alive. We designed a special device for acquiring high quality finger-vein images and propose a FPGA based VLSI platform to implement the finger-vein recognition system in the present study to achieve good recognition performance and reduce computational cost. The physical characteristics of a person like finger prints, hand geometry, face, voice and iris are known as biometric[1]

OVERVIEW OF THE SYSTEM

The system consists of three hardware system: Personal identification module, FPGA main board, and human-machine module. The personal identification is used to collect finger-vein images. The FPGA main board including the FPGA chip, memory (flash), and communication port is used to execute the finger-vein recognition algorithm based on DWT and communicate with the (PC) peripheral device. The human-machine communication module (LED) is used to display recognition results and receive inputs from users.



The proposed finger-vein recognition algorithm contains two modules: the enrollment person information and the finger vein verification stage. two stages start with vein image pre-processing, which includes detection of the Resize and crop process will be carried and enhancement also there. For the enrollment stage, after the pre-processing and the feature extraction step based on DWT feature, the finger-vein template database is built in server. For the verification stage, the input finger-vein image is matched with the corresponding template after its features are extracted and then matching based ED(near distance).its compared based nearby pixel comparison.

IMAGE ACQUISITION:

To get high quality near-infrared (NIR) images, a device special developed for acquiring the images of the finger-vein without being affected by temperature. The finger-vein patterns can be imaged based on the principle of light reflection or transmission of light. we stored those image and then only its processing Then normalized data is given to the Gabor filters. After that the extracted features are stored in template data base. [2]

Proposed algorithm:

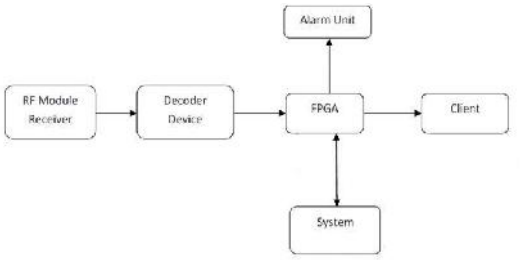
The proposed Input image will be having RF transmitter press and button .and then image will be selected. The segmented finger-vein image is then enhanced to improve its contrast. The vein image is resize the original image size, and enlarged back to its original image size. Next, the vein image is resize the original image size for recognition. The interpolation is used in this resizing procedure. Finally, equalization is used for enhancing the gray level contrast image.

Feature Extraction:

We have proposed the DWT and its local transformation from time and frequency and can be easily generate a variety of different resolutions. It decomposes the image into different sub band, namely, LL, LH, HL, and HH.

The high-frequency sub band contains edge information of input and LL sub band contains the clear information about the image. The two level of wavelet will be performed to represent an image and statistical feature energy is measured from all decomposed wavelet band to characterize the region.

Hardware section:



Euclidean Distance Matching:

Euclidean distance measures the similarity between two different feature vectors using (7).

$$ED = \sqrt{\sum_{j=0}^{J} (FV_{1,j} - FV_{2,j})^2} \qquad (7)$$

where J is the length of the feature vector, Fvi is the feature vector for individual.

FPGA : A Field-programmable Gate Array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence "field-programmable gate array". The FPGA configuration is specified using a hardware description language (HDL), similar to that used for an application-specific integrated circuit (ASIC). FPGAs is used to implement any logical function that an ASIC will perform. To update the functionality re-configuration of the portion of the design[1] and the low non-recurring engineering costs relative to an ASIC design, offer advantages for many **applications. FPGA's contain programmable logic** components are called "logic blocks", and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together"—somewhat like many (changeable) logic gates that can be inter-wired in (many) different configurations. The logic blocks can be configured to perform complex functions, or simple logic gates like XOR and AND. In FPGAs, the logic block includes memory devices, which may be simple flip-flops or most complete blocks of memory. The secret code is formed from middle row of the enhanced image. Then, it is converted to Hexadecimal code [4].

In addition to digital functions, some FPGAs have analog features. The most common analog feature is programmable slew rate and drive strength on each output pin, allowing the engineer to set slow rates on lightly loaded pins that would otherwise ring unacceptably, and to set stronger, faster rates on heavily loaded pins on high-speed channels that would otherwise run too slow. Another relatively common analog feature is differential comparators on input pins designed to be connected to differential signaling channels. A few "mixed signal FPGAs" have integrated peripheral Analog-to-Digital Converters (ADCs) and Digital-to-AnalogConverters (DACs) with analog signal conditioning blocks allowing them to operate as a system-on-a-chip. Such devices blur the line between an FPGA, which carries digital ones and zeros on its internal programmable interconnect fabric, and field-programmable analog array (FPAA), which carries analog values on its internal programmable interconnect fabric. A investigation has been performed to determine

the tradeoffs between security, and energy and to determine the secure partitioning between dongle and server[5]

RF Encoder and Decoder General Encoder and Decoder Operations

Transmission through RF is better than IR because of many reasons. Firstly, signals through RF can travel through larger distances making it suitable for long range applications. Also, while IR mostly operates in line-of-sight mode. RF signals can travel even when there is an obstruction between transmitter & receiver. Next, RF transmission is more strong and reliable than IR transmission. RF communication uses a specific frequency unlike IR signals which are affected by other IR emitting sources. This RF module comprises of an RF Transmitter and an RF Receiver. The transmitter/receiver pair operates at a frequency of 434 MHz An RF transmitter receives serial data and transmits it wirelessly through RF through its antenna connected at pin4. [6]The angle of the finger in the image re-quire some form of normalization, since these qualities will vary each time.The transmission occurs at the rate of 1Kbps - 10Kbps.The transmitted data is received by an RF receiver operating at the same frequency as that of the transmitter. The RF module is often used along with a pair of encoder/decoder. The encoder is used for encoding parallel data for transmission feed while reception is decoded by a decoder. HT12E-HT12D, HT640-HT648.

RF Transmitter:

Pin No	Function	Name
1	Ground (0V)	Ground
2	Serial data input pin	Data
3	Supply voltage; 5V	Vcc
4	Antenna output pin	ANT

RF Receiver

Pin No	Function	Name
1	Ground (0V)	Ground
2	Serial data output pin	Data
3	Linear output pin; not connected	NC
4	Supply voltage; 5V	Vcc
5	Supply voltage; 5V	Vcc
6	Ground (0V)	Ground
7	Ground (0V)	Ground
8	Antenna input pin	ANT

Controlling the Project with a FPGA and buzzer unit

Using these RF transmitter & receiver circuits with a FPGA would be simple. We can simply replace the switches used for selecting data on the HT-12E with the output pins of the FPGA. Output of FPGA is known

person means VB window will be get money and output of FPGA is unknown person means Buzzer unit on condition.

CONCLUSION

The present study proposed an finger-vein recognition system based on the DWT and VHDL implemented on a FPGA platform. The proposed system store capturing finger-vein images, a method for resize, crop and a novel method combining Wavelet features and for recognition. The images from dataset were taken over long time interval by a prototype device we built and its compared ED based on sample image and identifying known or unknown person and showed in hardware also low computational complexity and low power consumption.

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