An Efficient Memetic Algorithm to reduce Total Wire Length In Global Routing

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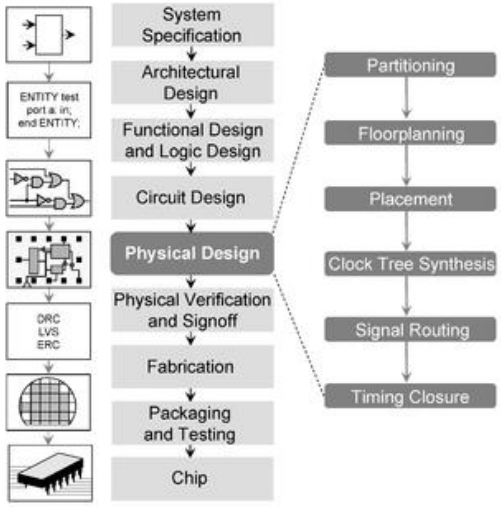
ABSTRACT

During recent years, the large problem space of VLSI circuits has led global routing to a NP complete one. In 2D ICs, this problem is more complex. The routing constraints are Minimize total wire length, Minimize knees in path, Meet timing budget. To overcome these problems Memetic algorithm has been used .It is the combination of Global and Local search this is used in many successful Hybrid optimization approaches. In Memetic Algorithms (MAs) local search is used to improve the fitness of individuals in the population. Memetic Algorithms is very effective in solving many hard combinatorial optimization problems. This algorithm combines Genetic Algorithms and advanced local search to solve VLSI circuit Routing.

Keywords: **VLSI physical design, Global routing, Wire Length Constrains, Benchmarks, Memetic Algorithm**

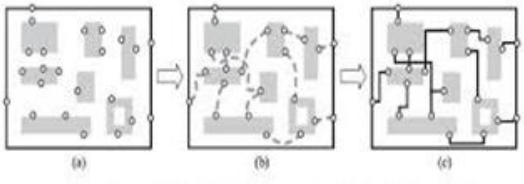
1.INTRODUCTION

VLSI physical design is the process of determining the physical location of active devices and interconnecting them inside the boundary of a VLSI chip. Since the cost of fabricating a circuit is a function of a circuit area, circuit layout techniques aim to produce layouts with a small area which implies fewer defects, hence a higher yield. Phases included in the physical design are partitioning, floor planning, placement and routing. Routing (global and detailed) problems must be solved to minimize the total chip area by reducing total wire length. The purpose of a global router is to decompose a large routing problem into small and manageable sub-problems (detailed routing). This decomposition is carried out by finding a rough path for each net in order to reduce the chip size, shorten wire length and evenly distribute the congestion over the routing area.



ROUTING PHASE

Routing is an important step in the design of Integrated circuits (ICs).It generates wiring to interconnect pins of the same signal, while obeying the manufacturing design rules. As IC process advances to nanometer technology, foundries may fabricate billions of transistors in a single chip, and the number of transistors per die will grow drastically. This increasing complexity imposes substantial challenges for physical design, especially for routing. Research in VLSI routing has received much attention in the literature. Routing is typically a very complex combinatorial problem. To make it manageable, the routing problem is usually solved by use of a two-stage approach of global routing followed by detailed routing. The global routing algorithm first partitions the routing region into tiles and assigns tile-to-tile paths for all nets while attempting to optimize some given objective function (e.g., total wirelength and circuit timing). Then, guided by the paths obtained in global routing, detailed routing assigns actual tracks and vias for nets.



(a) A given placement result with fixed location of blocks and pins

(b) Global routing
(c) Detailed routing

After placement, we have a placed information about the exact locations of blocks, pins of blocks, and I/O pads at chip boundaries. We are also provided with a netlist that describes a list of connections by indicating which pins or pads should be electrically connected to form a set of nets. First divide the routing region into tiles and then generate a "loose" route for each connection by finding the tile-to-tile paths to connect pins and/or pads.

WIRE LENGTH CONSTRAINTS

The global routing is an important step in VLSI physical design. Global routing with minimum wire length reduces the total cost of the circuit, reduces the propagation delay of signals and results in better electrical performance. However the global routing problem is NP-hard. The general global routing problems is of two types – line routing and maze routing. The two approaches are sequential and concurrent. In sequential approach the nets are routed one at a time. The order is dependent on factors like critically estimated wire length, etc. If further routing is impossible because some nets are blocked the nets routed earlier, apply Rip-Up and Re-route technique. The major drawback of sequential approach is that it suffers from net ordering problem. In concurrent approach all the nets are considered simultaneously. Thus it can be formulated as an integer program.

LAYOUT LAYERS AND DESIGN RULES

•Size rules, such as minimum width: The dimensions of any component (shape), e.g., length of a boundary edge or area of the shape, cannot be smaller than given minimum values. These values vary across different metal layers.
•Separation rules, such as minimum separation: Two shapes, either on the same layer or on adjacent layers, must be a minimum (rectilinear or Euclidean diagonal) distance apart.
•Overlap rules, such as minimum overlap: Two connected shapes on adjacent layers must have a certain amount of overlap due to inaccuracy of mask alignment to previously-made patterns on the wafer.

PHYSICAL DESIGN OPTIMISATIONS

•Technology constraints enable fabrication for a specific technology node and are derived from technology restrictions. Examples include minimum layout widths and spacing values between layout shapes.
•Electrical constraints ensure the desired electrical behavior of the design. Examples include meeting maximum timing constraints for signal delay and staying below maximum coupling capacitances.
•Geometry (design methodology) constraints are introduced to reduce the overall complexity of the design process. Examples include the use of preferred wiring directions during routing, and the placement of standard cells in rows.

PROBLEM DEFINITION

The problem definition for the general routing problem is as follows:

Inputs:

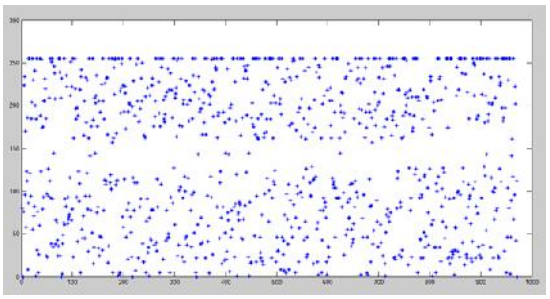
1. A placed layout with fixed locations of chip blocks, pins, and pads
2. A net list
3. A timing budget for each critical net
4. A set of design rules for manufacturing process, such as resistance, capacitance, and the wire/via width and spacing of each layer

Output:

Wire connection for each net presented by actual geometric layout objects that meet the design rules and optimize the given objective, if specified.

RESULT

In this paper, we identified the module locations from the standard ISPD '98 benchmarks circuits using MATLAB.



CONCLUSION

Thus the main aim of this paper is to reduce the total wire length in the routing region. We have identified the modules from the benchmark files using Matlab. Further, we will be connecting those modules using global routing and then Memetic algorithm will be used to find the global optimum solutions..

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