LAUNCH OFF SHIFT AND CAPTURE POWER REDUCTION IN TRANSITION FAULT TESTING BASED ON LOCAL SCAN ENABLE GENERATOR

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ABSTRACT

The electronic design automation method or technology is used to find an input (or test) sequence that, when applied to a digital circuit, enables automatic to distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects. A defect is an error caused in a device during manufacturing process. The generated patterns are used to test semiconductor devices after manufacture and in some cases to assist with determining the cause of failure. The output of a test pattern when testing a fault free device that works exactly as designed is called the expected output of the test pattern. The Transition fault model generation patterns are Launch-off shift and Launch-off capture methods. In existing method the controllability of launching a transition and the quality of results to be low. So here a novel scan based at speed test is proposed in which a transition can be launched either from the scan path or functional path. A new scan cell referred to as Local Scan Enable Generator(LSEG), is inserted in the scan chain to generate the local scan enable signals. The proposed method which provides the better test faults and improves the controllability.

INTRODUCTION

Microelectronics industry profitability is based on Moore's Law, which predicts an exponential decrease in feature size [1]. Hence, after four decades, integrated circuits became SoC (Systems on a Chip) with ever increasing complexity, density and performance. Such trend also enhanced power consumption, leading to the need of low-power design, and sophisticated power and thermal management solutions. In order to constraint internal electric fields (and constraint power consumption), for each node technology a reduction of the power supply voltage level, VDD, is required. Today's technologies (down to 65 nm, VDD=1 V, and hundred million gates operating in the GHz range) use new processing materials and manufacturing processes, like low-K and high-K dielectric materials and OPC (Optical Proximity Correction) [2]. New materials and processing technology lead to new, emerging physical defects. Complexity, performance, power consumption and low pin count bring a difficult challenge: how to specify and run a cost-effective test process [1]. In fact, for digital systems, not only it is difficult to derive a cost-effective test to cover static faults (like those described e.g. by the classic single Line-Stuck-At (LSA) fault model), but also dynamic faults, as a significant set of emerging defects manifest themselves only as time-related defects. Hence, cost-effective solutions to uncover dynamic faults (namely, delay faults) became mandatory [3]. Delay test quests for two-vector sequences, the first vector to initialize the circuit, and the second vector to trigger a transition and/or the activation of a Boolean difference through a propagation path to an observable output.

As a matter of fact, testing is crucial in product life-cycle. First, in the design environment, test is used in design Second, in the manufacturing environment, test must uncover manufacturing defects, discriminating good from defective parts. In this respect, it is usual to define the product Defect Level, as the percentage of defective parts that pass successfully the production test. Typical Defect Level values, for quality products, are today in the range of 10-1 ppm (parts per million). Some defects lead to incorrect Boolean functionality; others lead only to incorrect performance (timing) of the system. Third, during product lifetime, for many products it is necessary to detect any defects that can produce a failure operation of the system.

Usually, the following attributes (and corresponding metrics) are used for test

- Test effectiveness (TE) – the ability of the test pattern to uncover the likely physical defects which may occur in production, or during product lifetime.
- TE is usually measured by the fault coverage, the percentage of listed faults that are uncovered by the

test pattern. This metrics depends on the test pattern and on the fault model used to describe the impact of the physical defect on circuit behaviour.

- Test Length (TL) – the number of individual test vectors in the test pattern. This value is relevant, as the test application time is directly proportional to TL and the clock period. It also has impact on test development costs, as the test pattern generation process costs depends on TL.

- Test Overhead (TO) – the additional cost associated with the implementation of test functionality built in the SoC. It is usually measured by the percentage Si area overhead, and clock frequency decrease due to test. It is also measured by the increase in pin count.

- Test Power (TP) – the power consumption (average and peak) associated with the test sessions. Structural test normally requires high node toggling, leading to high power dissipation in test mode. It is usually measured by the weighted switching activity of the circuit nodes in CMOS.

The transition fault and path delay fault testing together provide a relatively good coverage for delay-induced defects [6] [7]. Path delay model targets the cumulative delay through the entire list of gates in a pre-defined path while the transition fault model targets each gate output in the design for a *slow to rise* and *slow-to-fall* delay fault [8]. Transition fault testing is widely practiced in industry due mainly to its manageable fault count (two faults in each gate) and availability of commercial tools. To test a transition fault, a pattern first is applied to initialize the circuit and another pattern is applied to apply a transition at a target gate terminal. The response is observed at the outputs of the circuit under test (CUT). Scan-based structural tests generated by an automatic test pattern generator (ATPG) are increasingly used as a cost-effective alternative to the at-speed functional pattern approach [5] [9].

To perform a scan-based transition fault test, a pattern pair($V1$,$V2$) is applied to the circuit-under-test. Pattern $V1$ is termed as the initialization pattern and$V2$ as the launch pattern. $V2$ launches the signal transition (0 to 1 or 1 to 0) at the desired node. It also helps propagate the output transition to the output of CUT (scan flip-flops or primary outputs). The response of the CUT to the pattern $V2$ must be captured at functional speed (rated clock period). The whole operation can be divided into 3 cycles:

1) Initialization Cycle (IC), where the CUT is initialized to a particular state ($V1$ is applied),
2) Launch Cycle (LC), where a transition is launched at the target gate terminal ($V2$ is applied) and
3) Capture Cycle (CC), where the transition is propagated and captured at an observable point.

Various scan-based transition fault testing methods were proposed in literature [10] [11] [12]. Depending on how the transition is launched and captured, there are three transition fault pattern generation methods called *launch-off-shift*, *launch-offcapture*, and *enhanced-scan*.

In the first method, referred to as *launch-off-shift* (LOS) [10], the transition at the gate output is launched in the last shift cycle during the shift operation. Figure 1(a) shows the path of transition launch in LOS method for a multiplexed-DFF design; similar approach can be applied to an LSSD. The transition is launched from the scan-in pin (SD) of any flip-flop in the scan chain. This activates the required transition at the target gate terminal which is propagated and captured through the functional path at an observable point (D) of any flip-flop in the scan chain.

The LC is a part of the shift operation and is immediately followed by a fast capture pulse. The scan enable (SEN) signal is high during the last shift and must go low to capture the response at the CC clock egde. The time period for SEN to make this 1 to 0 transition corresponds to the functional frequency. Hence, LOS requires the SEN signal to be timing critical. Skewing the clock (CLK) creates a higher launch-tocapture clock frequency than standard shift clock frequency. Saxena et al. [13] list more launch-off-shift approaches

In *launch-off-capture* (LOC) method [11] the transition is launched and captured through the functional pin (D) of any flip-flop in the scan chain. Since, the launch pattern $V2$ depends on the functional response of the initialization vector $V1$, the launch path is less controllable due to which the test coverage is low. Figure 2(b) shows the waveforms of the LOC method in which the launch cycle is separated from the shift operation. At the end of scan-in (shift mode), pattern $V1$ is applied and CUT is set to an initialized state. A pair of at-speed clock pulses is applied to launch and capture the transition at the target gate terminal. This relaxes the at-speed constraint on the SEN signal and dead cycles are added after the last shift to provide enough time for the SEN signal to settle low.

The third technique, known as *enhanced scan* [12] requires that two vectors $V1$ and $V2$ are shifted into the scan flip-flops simultaneously. The main advantage of this technique is that it

simplifies ATPG and offers better coverage for both LOC and LOS techniques, since it eliminates any dependency between *V*2 and *V*1. Enhanced scan can also have a beneficial impact on test data volume, since more compact test patterns can be generated. The drawback on enhanced scan is that it needs hold-scan flops and is area-intensive, making it unattractive for ASIC designs. Enhanced scan using hold-scan flops has been used in high-performance microprocessors where the area overhead of the technique is justified.

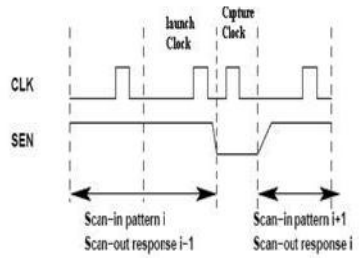
The LOS method is preferable from ATPG complexity and pattern count view points when compared to LOC method. In case of LOC, a high fault coverage cannot be guaranteed due to the correlation between the two patterns, *V*1 and *V*2. As the design size increases, the SEN fanout exceeds any other net in the design. The LOS constraints SEN to be timing critical which makes it difficult to implement using low cost testers and on designs where the turn-around-time is critical [15]. That is the main reason that LOC method has been widely practiced, especially on low cost testers [9]. Note that no at-speed SEN signal is required for LOC method.

Techniques are required to improve the LOC method's fault coverage. In this paper, we propose a technique to improve the fault coverage and reduce the pattern count by using an enhanced LOC technique. It intelligently selects a subset of scan cells to be controlled by LOC technique and the rest as scanpath. This improves the controllability of scan cells and detects some of the hard-to-detect-by-LOC faults.

Several techniques have been proposed to improve the LOS fault coverage but there has not been much work on the LOCmethod to the best of our knowledge. In [14], a hybrid scan architecture is proposed which controls a small subset of selected scan cells by LOS and the rest are controlled by LOC approach. A fast scan enable signal generator is designed which drives the LOS controlled scan flops. The ATPG method used is complex and current commercial tools do not support such a technique. Moreover, the selection criteria of the LOS controlled scan flops determines the effectiveness of the method. In some cases, the number of patterns generated by the hybrid method exceeds the LOC pattern count.
The implementation of LOS method using low cost testers is presented in [15]. A local at-speed scan enable signal is generated using a slow enable signal generated by a low cost tester. A local scan enable generator is designed; it can be inserted anywhere in scan chain and the launch and capture information are encapsulated in test data and transferred into the scan chain. The proposed technique in [15] focuses only on LOS and its implementation on low cost testers. The technique has no impact on fault coverage and pattern count.

Launch-off-Shift Method (LOS):

In launch-off-shift (LOS) approach [7], the transition at the gate output is launched in the last shift cycle during the shift operation. Figure 1.8 shows the launchoff- shift method waveform. The launch clock is a part of the shift operation and is immediately followed by a fast capture pulse. The scan enable (SEN) is high during the last shift and must go low to enable response capture at the capture clock edge. Since the capture clock is applied at the full system clock speed after the launch clock, the scan enable signal, which typically drives all scan flip-flops in the CUT, should also switch in the full system clock cycle. This requires the scan enable signal to be driven by a sophisticated buffer tree or strong clock buffer. Such a design requirement is often too costly to meet.



Waveform for LOC

Launch-off-Capture Method (LOC)

In the launch-off-capture approach [8], the launch cycle is separated from the shift operation. Figure 1.9 shows the waveforms of the launch-off-capture (LOC) method. At the end of scan-in (shift mode), pattern V1 is applied and CUT is set to an initialized state. A pair of at-speed clock pulses is applied to launch and capture the transition at the target gate terminal. This relaxes the at-speed constraint on the scan enable (SEN) signal and dead cycles are added after the last shift to provide enough time for the SEN signal to settle low. The launch-off-shift method is more preferable based on the ATPG complexity and pattern count compared to LOC method. The LOC technique is based on a sequential ATPG algorithm, while the LOS method uses a combinational ATPG algorithm. This will

increase the test pattern generation time in case of LOC, and also, a high fault coverage cannot be guaranteed due to the correlation between the two patterns, V1 and V2; note that V2 is the functional response of pattern V1. The main concern about the LOS is its requirement to at-speed SEN signal.

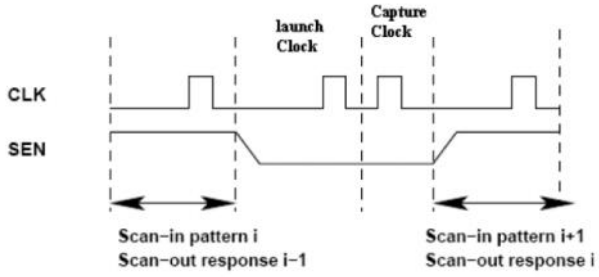


Figure 1.9: Waveform for Launch-off-Capture delay test

A. Contribution and Paper organization

In this paper, we propose a novel transition fault pattern generation technique called Enhanced LOC (ELOC). In this technique, the transition launch path is deterministically determined either through a *functional path* or a em scan path. This improves
the controllability of scan chains, increases the fault coverage, reduces the pattern count. A new scan cell, called local scan enable generator (LSEG), generates the local scan enable signals (not at-speed), used to control the scan chain mode of operation. A subset of scan chains are used as functional paths (like conventional LOC) and the rest are used as scan paths. This is controlled by scan enable signal; note that depending on how the scan enable signal changes during the launch and capture cycle the scan chain will be controlled either as functional path or scan path only. In a functional path, pattern*V*2 is generated using the functional response of pattern *V*1. In scan path, the pattern *V*2 is generated using the last shift but the responses are not captured using that scan chain. The scan enable control information for the launch and capture cycle is embedded in the test data itself. The LSEG cell has the flexibility to be inserted anywhere in the scan chain and the hardware area overhead is negligible.

II. ENHANCED LAUNCH-OFF-CAPTURE

The LOC method utilizes the functional response of the circuit to launch the transition at a target gate terminal and propagate the fault effect to an observable point. Launching a transition through functional response is difficult due to controllability issues. We now explain the controllability of LOC and describe how the LOC's test coverage can be improved by increasing its controllability.

LOCAL SCAN ENABLE SIGNAL (LSEN) GENERATION

The enhanced LOC method provides more controllability to launch a transition but requires independent scan enable signal for each scan chain. Multiple SEN ports can be used, but this increases the number of pins. The scan enable control information for all the scan chains differ only during the launch and capture cycles of the pattern. Hence, the scan enable signal from the external tester can be utilized for the scan shift operation and the scan enable control information for only the launch and capture cycles can be generated internally. The local
scan enable generator cells are inserted within the scan chains. Therefore, the control information is to be passed as part of the test data. The scan enable control information will be part of each test pattern and is stored in the tester's memory.

The normal scan architecture with a single scan enable signal from the external tester is shown in Figure 6(a). There are eight scan flip-flops in the scan chain and the test pattern shifted is 10100110. The external scan enable signal from the tester is referred to as the global scan enable (GSEN). Figure 6(b) shows the same circuit in which a local scan enable signal is generated from the test pattern data for the enhanced LOC method. The internally generated scan enable signal is termed as local scan enable (LSEN). The main objective is to de-assert GSEN after the entire shift operation and then generate the LSEN signal during the launch and capture cycle from the test data. In this case, the pattern shifted is modified to 1010[C]0110, where *C* is the scan enable control bit which is stored in scan flip-flop *A* at the end of the scan operation.

One extra scan flip-flop (A) and an OR-gate are added for the generation of LSEN signal. The output of A is ORed with GSEN to generate the LSEN signal (see Figure 6(b)). Note that GSEN is not an at speed signal. The GSEN signal asynchronously controls the shift operation. The values of the scan flip-flops during the various shift cycles are shown under each flip-flop. GSEN is de-asserted after the nth shift (IC) cycle, where n=9. n is the length of scan chain after inserting new cell A. After the GSEN signal is de-asserted at the end of the shift operation, the scan enable control during the launch and capture
cycles is the control bit C stored in A. At the end of the capture cycle, the LSEN signal is asynchronously set to 1 by GSEN for scanning out the response.

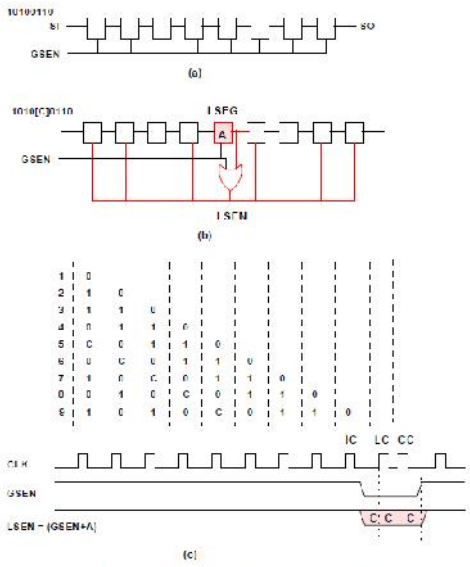


Figure 6. (a) Scan chain architecture, (b) Local scan enable (LSEN) generation and (c) LSEN generation process.

$$LSEN = (GSEN + A) = \begin{cases} 1 & \text{if GSEN=1} \\ A & \text{if GSEN=0} \end{cases}$$

Local Scan Enable Generator (LSEG)

During the launch and capture cycles of the pattern, the control bit shifted into scan flop *A* is used as the scan enable control. Figure 7 shows the LSEG cell architecture. It consists of a single flop which is used to load the control information required for the launch and capture cycles. The port definition is similar to a scan cell and the output of the flop is fed back to the functional input port of the flip flop. It consists of a scan-in (*SENin*) pin which takes GSEN signal as input. An additional scan-out (*SENout*) pin (*GSEN _ Q*) represents the LSEN signal. Therefore, after going to a control state *(C)* at the end of the shift operation (GSEN is de-asserted), LSEN remains in this state as long as it is asynchronously set to 1 by GSEN.

Table I shows the different modes of operation of LSEG cell. *GSEN*=1 represents the normal shift operation of the pattern. When *GSEN=0* and *C*=1, *LSEN*=1 and the scan chain acts in the shift mode to launch the transitions (*Shift-Launch* mode). The scan chain acts in the conventional LOC method when *GSEN=0* and *C*=0 (*Functional-Launch* mode). Note
that the LSEG cell can be inserted anywhere in the scan chain and it is not connected to the CUT. Hence, it has no impact on the functional timing and the CUT fault coverage.

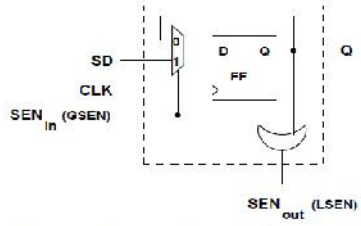
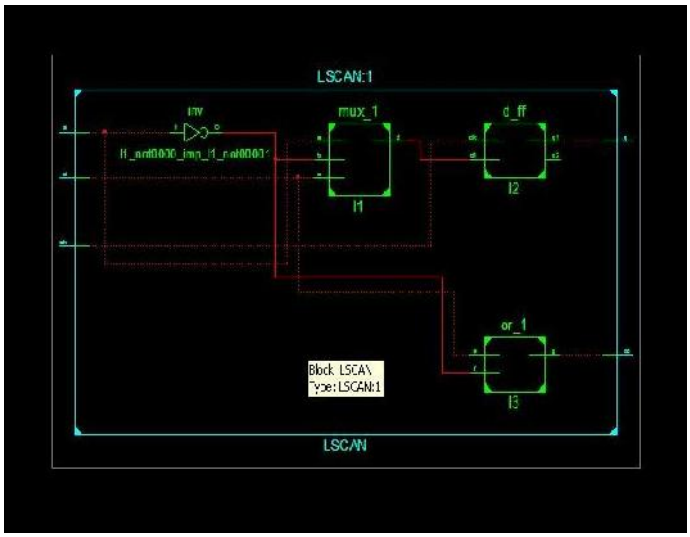


Figure 7 Local scan enable generator (LSEG) cell

TABLE I
LSEG OPERATION

GSEN	FF	LSEN	Operation
1	X	1	Shift
0	1	1	Shift-Launch
0	0	0	Functional-Launch

The LSEG cell provides a simple mechanism to generate the local internal scan enable signals. But, it has a shift dependency for the following flop in the shift register mode. If C=1, the LSEG flip-flop is constant at 1 for the launch and capture cycles and the flip-flop following the LSEG cell can generate only a 0 to 1 transition at its output. This may result in loss of coverage for faults which are in the logic cone and require a 1 to 0 transition on the flip-flop following the LSEG cell. In order to avoid loss of coverage without significant change in the architecture, the LSEG cell is modified such that the LSEG cell when loaded with the control bit, the cell will remain in this state and it is not in the shift path during the launch and capture cycles for C= 1. Figure 8 shows the modified LSEG cell architecture. It consists of an additional multiplexer and it does not
impact the functional path timing. When GSEN= 0, the LSEG cell is by-passed and the SD pin is directly connected to Q. In the Shift-Launch mode, the value from the previous flip-flop of LSEG cell is shifted into its following flip-flop.



C. LSEG Insertion Flow

There are two issues relating to insertion of multiple LSEG cells, 1) the number of LSEG cells, 2) insertion flow of LSEG cells (module level or top-level). If there is a large difference between the fault coverage between ELOC and LOS, then one reason might be that there is a large number of capture dependency faults in the design. The capture dependency can be broken by re-arranging the scan flip-flops between the scan chains. Since, the scan insertion tool is not aware of the LSEG methodology, the test engineer should analyze the capture dependency untestable faults and determine the number of LSEG cells to be inserted. For this particular design, we experimented by inserting three LSEG cells and the ELOC method gave about 2.3% higher fault coverage than LOC compared to 1.9% percent coverage improvement for one LSEG cell per scan chain. Moreover, the LSEG insertion method is not affected by re-ordering of the scan flip-flops during the physical design.

VI. EXPERIMENTAL RESULTS

We have experimented on eight industrial designs and Table IV shows the characteristics of these designs. In all designs, each scan chain is inserted with one LSEG cell. The total transition faults are shown in column *TF*. During ATPG, the faults related to clocks, scan-enable and set/reset pins, referred to as untestable faults (*UF*), are not added to the fault list. The clock related faults can only be detected by implication and the remaining faults (scan-enable/set/reset) are untestable as the signals remain unchanged during the launch and capture cycles

These faults contribute approximately 10-15% of the total transition faults. The total transition faults excluding *UF* faults is used as the real fault (*RF*) set during pattern generation. Table V shows the ATPG results comparing LOC and ELOC methods. The DT, FC, # Patt columns shows the detected faults, the fault coverage percentage and the number of patterns generate respectively for each method. Note that the CPU time for ELOC method is greater than LOC method since the tool has to do additional processing to find the transition launch activation path. The DT are the extra faults detected by the ELOC method. The ELOC method provides higher fault coverage upto 1.87% (*FC*) compared to LOC method and also for a given fault coverage, the number of patterns generated by ELOC is less in all designs. The (*Patt*) column is the percentage pattern reduction for the maximum fault coverage achieved by LOC method. Figure 22 shows the number of patterns in both methods for the highest LOC fault coverage achieved. In all cases the ELOC method generates a smaller pattern set as the controllability of transition launch has increased.

$$\Delta Patt = \{\frac{LOC - ELOC}{LOC}\} FC_{LOC_{max}}$$

The LSEG-based solution provides better fault coverage and pattern count with a simple addition of a LSEG cell controlling the scan path. On an average, the ELOC gives 0.72% higher fault coverage compared to conventional LOC method. The fault coverage of ELOC method can be increased further by careful scan insertion. Presently, the scan insertion tool stitches the scan cells based on the lexical naming convention of the scan flops. The best results in terms of fault coverage can be obtained, if the scan insertion tools can stitch the chains such that the inter-scan chain faults are increased. However, irrespective of scan chain order, the pattern volume reduction is achieved due to improved controllability.

VII. CONCLUSION

In this paper, a new method of transition fault testing, referred as *enhanced launch-off-capture*, has been proposed which provides better controllability than the conventional launch-off-capture method. LOC testing is known to provide less quality results, both in terms of pattern count and fault coverage, but design teams may not use launch-off-shift due to the challenge of routing the scan enable signal. Our solution is to generate local scan-enable signals that control the transition launch path; for this purpose, we rely on embedding some scan enable control information in the patterns. We use a

special cell called the LSEG cell for the generation of the local scan enable signal. This cell is simple to design and layout, and its area overhead is comparable to that of a scan flop. The number of LSEG cells inserted in the design will be small, thereby making the area overhead due to our technique negligible. The LSEG-based solution provides greater flexibility and controllability for transition fault pattern generation. The DFT insertion and ATPG can be easily performed using the commercial ATPG tools; therefore our solution is easy to practice.

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