SINGLE ENDED ENERGY RECOVERY FLIPFLOP DESIGN BASED ON CONDITIONAL DISCHARGE TECHNIQUE

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ABSTRACT: The choice of flip-flop technologies is an important importance in style of VLSI integrated circuits for top speed and high performance CMOS circuits. The most objective of this project is to style a Low-Power Pulse-Triggered flip-flop. Single complete Energy Recovery Flip-Flop is one quite Energy Recovery Flip-Flop. wherever Energy Recovery may be a technique developed for low power digital circuits, the energy recovery circuit achieves low energy dissipation by proscribing current to flow across device with low dip associated by employment the energy keep on their capacitors by victimization an AC sort offer voltage. This SCCER Flip-Flop uses the Conditional Discharge Technique. They accommodate most of the ability that has been applied to the chip. Flip-flop is one among the foremost power consumption parts. It's vital to scale back the ability dissipation in each clock distribution networks and flip-flops. the ability delay is especially attributable to the clock delays. The delay of the flip-flops ought to be decreased for economical implementation

I.INTRODUCTION

Flip-flops (FFs) area unit the fundamental storage parts used extensively altogether sorts of digital styles .One latch or Flip-Flop will store one little bit of data. the most distinction between latches and flip-flops is that for latches, their outputs area unit perpetually littered with their inputs as long because the alter signal is declared. In different words, once they area unit enabled, their content modifications directly once their input change. Flip-flops, on the opposite hand, have their content modification solely either at the rising or falling fringe of the alter signal. This alter signal is typically the dominant clock signal. Once the rising or falling fringe of the clock, the flip-flop content remains constant even. There area unit primarily four main kinds of latches and flip-flops: SR, D, JK, and T. the key variations in these flip-flop [13] varieties area unit the quantity of inputs they need and the way they modify state. for every sort, there are totally different variations that enhance their operations. Figure 1(a), (b) illustrates the

Distinction between positive edge triggered flip flop and an energetic high latch. Because it are often seen during this figure, doable changes of input are often seen at the output of the latch whereas it's clear

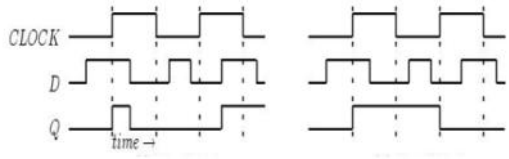

Fig 1
(a) Active High latch (b) Positive Edge Triggered Flip-Flop

The performance of a flip-flop is measured by 3 necessary timings and delays: propagation delay (Clock-to-Output), setup time and hold time. They mirror within the system level performance of the Flip-Flops [5]. Setup time and hold time outline the link between the clock and computer file as shown within the Figure 1(c).Setup time and hold time describe the temporal arrangement needs on the D input of a Flip-Flop with relevancy the Clk input. Setup and hold time outline a window of your time that the D input should be valid and stable so as to assure valid knowledge on the letter of the alphabet output. Setup Time (Tsu) Setup time is that the time that the D input should be valid before the Flip-Flop samples. Hold Time (Th) – Hold time is that the time that D input

should be maintained valid when the Flip-Flop samples. Propagation Delay (Tpd) – Propagation delay is that the time that takes to the sampled D input to propagate to the letter of the alphabet output."

This paper is organized as follows. Section II describes the technique accustomed cut back the change activity within flip-flops, and it introduces the new technique. Section III describes the specific pulse-triggered flip-flop, and the associated limitations. Section IV presents the new flip-flop utilizing the new technique for low-power and high-speed styles. Section V compares flip-flops and shows the conclusion.

II. MECHANISM FOR REDUCING SWITCHING ACTIVITY

The clock-gating in the conditional capture technique results in redundant power consumed by the gate controlling the delivery of the delayed clock to the flip-flop. As a result, conditional pre-charge technique outperformed the conditional capture technique in reducing the flip-flop EDP [16]. But the conditional pre-charge technique has been applied only to imp-FF, and it is difficult to use a double-edge triggering mechanism for these flip-flops, as it will require a lot of transistors. A new technique, Conditional discharge technique is suitable for both implicit and explicit pulse-triggered flip-flops without the problems associated with the conditional capture technique.

A new technique, conditional discharge technique, is proposed in this paper for single ended conditional capturing energy recovery flip-flop. Also, this new technique is employed to present a new flip-flop as well (Section IV). In this technique, the extra switching activity is eliminated by controlling the discharge path when the input is stable HIGH and, thus, the name Conditional Discharge Technique. In this scheme, an nMOS transistor controlled Qb by is inserted in the discharge path of the stage with the high-switching activity. When the input undergoes a LOW-to-HIGH transition, the output Q changes to HIGH and Qb to LOW. This transition at the output switches off the discharge path of the first stage to prevent it from discharging or doing evaluation in succeeding cycles as long as the input is stable HIGH.

III.EXISTING METHOD

The design conjointly employs a static latch structure and a conditional pre-charge theme to avoid superfluous switch at an enclosed node. However, there square measure 3 major variations that result in a singular TSPC latch structure and build the planned style distinct from the previous one. First, a weak pull-up pMOS semiconductor unit MP1 with gate connected to the bottom is employed within the 1st stage of the TSPC latch. this offers rise to a pseudo-nMOS logic vogue style, and also the charge keeper circuit for the inner node X will be saved. Additionally to the circuit simplicity, this approach conjointly reduces the load capacitance of node X [20], [21]. Second, a pass semiconductor unit MNx controlled by the heartbeat clock is enclosed in order that input file will drive node letter of the latch directly (the signal feed-through scheme). Alongside the pull-up semiconductor unit MP2 at the second stage electrical converter of the TSPC Latch, this further passage facilitates auxiliary signal driving from the input supply to node letter. The node level will therefore be quickly force up to shorten the info transition delay. Third, the pull-down network of the

Second stage electrical converter is totally removed. Instead, the recently used pass semiconductor unit MNx provides a discharging path. The role vie by MNx is therefore twofold, i.e., providing further driving to node letter throughout zero to one information transitions, and discharging node Q throughout “1” to “0” information transitions. Compared with the latch structure employed in SCDFF style, the circuit savings of this style embody a charge keeper (two inverters), a pull-down network (two nMOS transistors), and a sway electrical converter. the sole additional part introduced is AN nMOS pass semiconductor unit to support signal feed through.

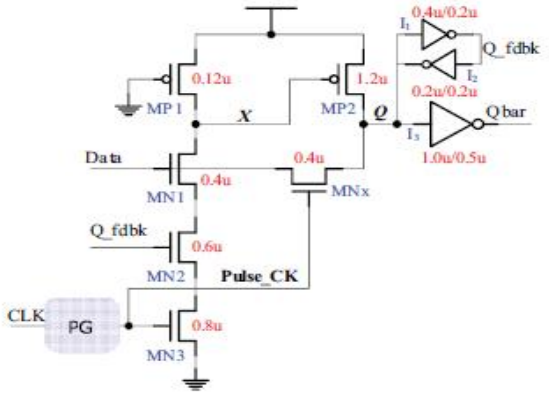

Fig.2. Schematic of the pulse triggered flip-flop design

This theme really improves the “0” to “1” delay and therefore reduces the inequality between the increase time and also the fall time delays. compared with different P-FF styles like ep-DCO, CDFF, and SCDFF, the planned style shows the foremost balanced delay behaviors. The principles of FF operations of the planned style ar explained as follows. once a clock pulse arrives, if no knowledge transition happens, i.e., the computer file and node letter of the alphabet ar at an equivalent level, on current passes through the pass semiconductor device MNx, that keeps the input stage of the FF from any driving effort. At an equivalent time, the computer file and also the output feedback Q_fdbk assume complementary signal levels and also the pull-down path of node X is off. Therefore, no signal switch happens in any internal nodes. On the opposite hand, if a “0” to “1” knowledge transition happens, node X is discharged to show on semiconductor device MP2, that then pulls node letter of the alphabet high. Relating Fig. 2(b), this corresponds to the worst case temporal order of the FF operations because the discharging path conducts just for a pulse period. However, with the signal feed through theme, a lift is obtained from the input supply via the pass semiconductor device MNx and also the delay is greatly shortened. Though this looks to burden the input supply with direct charging/discharging responsibility, that could be a common pitfall of all pass semiconductor device logic, the state of affairs is completely different during this case as a result of MNx conducts just for a really short amount. Relating Fig. 2, once a “1” to “0” knowledge transition happens, semiconductor device MNx is likewise turned on by the clock pulse and node letter of the alphabet is discharged by the input stage through this route. not like the case of “0” to “1” knowledge transition, the input supply bears the only real discharging responsibility. Since MNx is turned on for less than a brief time interval, the loading impact to the input supply isn't vital. particularly, this discharging doesn't correspond to the vital path delay and concerns no semiconductor device size tweaking to boost the speed. additionally, since a keeper logic is placed at node letter of the alphabet, the discharging duty of the input supply is upraised once the state of the keeper logic is inverted.

IV.PROPOSED METHOD

Single Ended Energy Recovery Flip-Flop(SER) is one quite Energy Recovery Flip-Flop. wherever Energy Recovery could be a technique developed for low power digital circuits, the energy recovery circuit achieves low energy dissipation by proscribing current to flow across device with low dip associated by employment the energy hold on their capacitors by victimization an AC kind offer voltage. This SCCER Flip-Flop uses the Conditional Discharge Technique

A.OPERATION OF PLANNED METHODOLOGY

SCCER is that the refined Low power pulse triggered flip-flop the circuit diagram of SER is shown within the below figure three. This SER Flip-Flop uses the Conditional Discharge Technique. during this technique, the additional change activity is eliminated by dominant the discharge path once the input is stable HIGH and therefore the name conditional discharge technique. during this theme, associate NMOS junction transistor controlled by QB is inserted within the discharge path of the stage with high change activity. once the input undergoes a Low-to-High transition the output letter changes to high and QB to low. This transition at the output switches off the discharge path of the primary stage to forestall it from discharging. during this style, a weak pull up junction transistor P1 is used in conjunction with associate electrical converter I2 to cut back the load capacitance of node. The discharge path contains NMOS transistors N2 and N1 connected nonparallel. so as to eliminate superfluous change at node X, an additional NMOS junction transistor N3 is used. Since N3 is controlled by Q_fdbk, no discharge happens if computer file remains high.

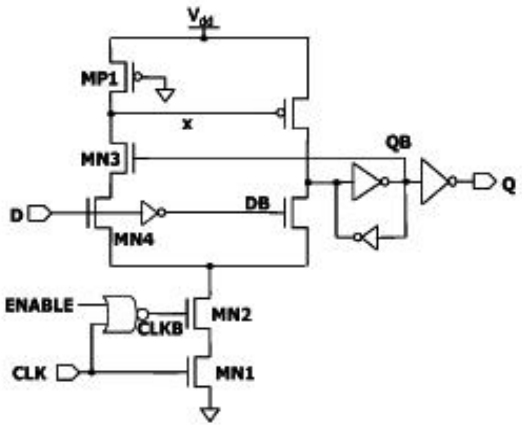

Fig.3. Circuit diagram of Single ended energy recovery flip-flop

Energy recovery is the promising techniques designed by adiabatic logic and consumes less power over conventional CMOS based logic. The advantage SER is to ensure that there is no internal redundant switching on SET and RESET nodes if input data remains idle for long time. Therefore, power consumption is minimized for low data switching activities

B. SER WITH SELF CONTROLLABLE VOLTAGE LEVEL CIRCUIT LOGIC (SVL)

The SVL circuit will cut back stand by outpouring power of CMOS logic circuits with least overheads in terms of chip space and speed. within the operative Mode, it provides high-Speed Operation for load circuits.

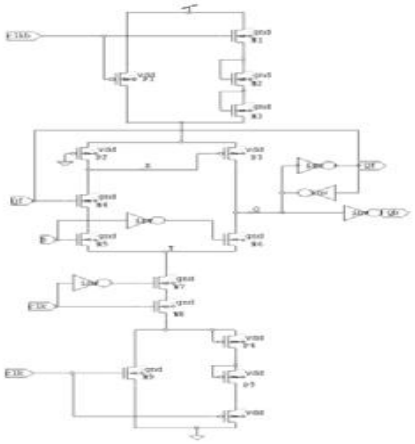

Fig.4.Circuit Diagram for SER with SVL logic

The SVL logic is more to the higher half and therefore the lower a part of the changed SER circuit. The changed SER circuit is small in semiconductor count when put next to work half dozen.

C.SCCER WITH SELF-ADJUSTABLE VOLTAGE LEVEL CIRCUIT (SAL) LOGIC

It's necessary to cut back the leak power altogether transportable systems. Self-adjustable voltage level logic may be a technique that is employed for reducing leak power within the circuit [13].

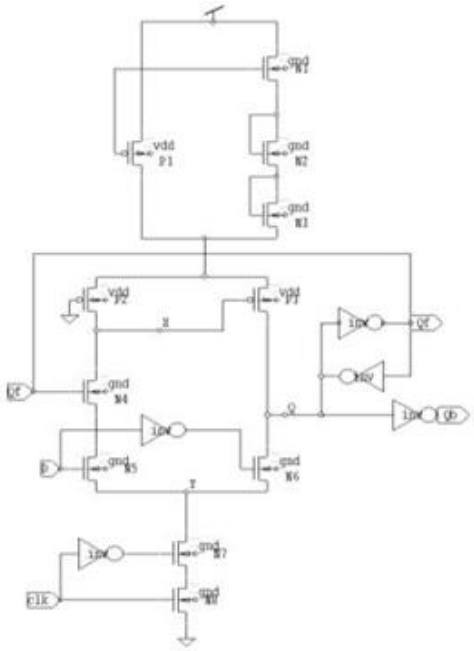

Fig.5.Circuit Diagram for SER with SAL logic

In the figure the SAL logic is another on the highest most a part of the changed SER circuit and also the circuit behaves as D flip-flop

V.CONCLUSION

In this paper, a replacement technique, conditional discharge, is introduced to scale back the switch activity of some internal nodes in flip-flops. this method was used in a very new flip-flop, conditional discharge flip-flop. the new flip-flop will save the energy with the high speed than the pulse triggered flip-flop. so as to get correct results, we've got simulated the circuits in a very real setting, that dictates that the flip-flops' inputs (clock, data) area unit driven by fastened input buffers, and therefore the outputs area unit needed to drive Associate in Nursing output load. The comparison of low power pulse triggered flip-flops with SAL ,SVL logics is applied and therefore the best power -delay-performance is obtained.

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