Design of high speed Dynamic Dual rail double tail latch Comparator

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Abstract: - Modern communication and signal processing is dependent on the high speed and low power consumption of the Analog-to-Digital converters (ADC) to a very large extent. Comparator is the basic building block of the ADCs which compares the two set of variables and change the input analog signal in digital. In this paper a new design of double tail comparator is proposed for high frequency of data conversion and is compared with the best available recently proposed double tail comparator design in term of area on chip power utilization, delay consideration. The proposed topology is based on two cross coupled differential pairs positive feedback and switchable current sources, has a lower power dissipation, higher speed, less area, and it is shown to be very robust against transistor mismatch, noise immunity. A new CMOS dynamic comparator using dual input single output differential amplifier as latch stage suitable for high speed analog-to-digital converters with High Speed, low power dissipation and immune to noise. This topology completely removes the noise that is present in the input. The structure shows lower power dissipation and higher speed than the conventional comparators.

I.INTRODUCTION

Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to digital converters (ADCs), memory sense amplifiers (SAs) and data receivers. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time. However, an input-referred latch offset voltage, resulting from static mismatches such as threshold voltage Vth and *!Cox* variations in the regenerative latch, deteriorates the accuracy of such comparators. Moreover, dynamic mismatch from the unbalanced parasitic capacitances on the output nodes of the latch causes the additional offset term during evaluation phase [5], [6]. Because of this reason, the input referred latch offset voltage is one of the most important design parameters of the latched
comparator. If large devices are used for the latching stage, a low offset can be achieved at the cost of the reduced speed due to slowing the regeneration time and the increased power dissipation. More practically, the input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output latch stage as shown in Figure1. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage. However, the preamplifier based comparators suffer not only from large power consumption for a large bandwidth but also

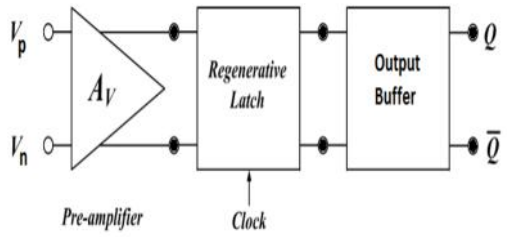

Figure 1 Typical block diagram of a high-speed voltage comparator

from the reduced intrinsic gain with a reduction of the drain-to-source resistance *rds* due to the continuous technology scaling [7]. In this paper, we present a new dynamic latched comparator which shows lower input-referred latch offset voltage and higher load drivability than the conventional dynamic latched comparators. With two additional inverters inserted between the input- and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage was improved and the complementary version of the output-latch stage, which has bigger output drive current capability at the same area, was implemented.

The remaining sections of the paper are organized as follows. Section II provides an overview of the previous works about the dynamic comparators in terms of their advantages and drawbacks, and section III describes the proposed dual rail dynamic latched comparator which is based on the structures from [3], [4]. Results from PSPICE with *VDD*=1V presented in Section IV and conclusion is present in Section V.

II. DYNAMIC COMPARATORS

Clocked regenerative comparators have found wide applications in many high-speed ADCs since they can make fast decisions due to the strong positive feedback in the regenerative latch. Recently, many comprehensive analyses have been presented, which investigate the performance of

these comparators from different aspects, such as noise [11], offset [12], [13], and [14], random decision errors [15], and kick-back noise [16]. In this section, a comprehensive delay analysis is presented; the delay time of two common structures, i.e., conventional dynamic comparator and conventional dynamic double-tail comparator are analyzed, based on which the proposed comparator will be presented.

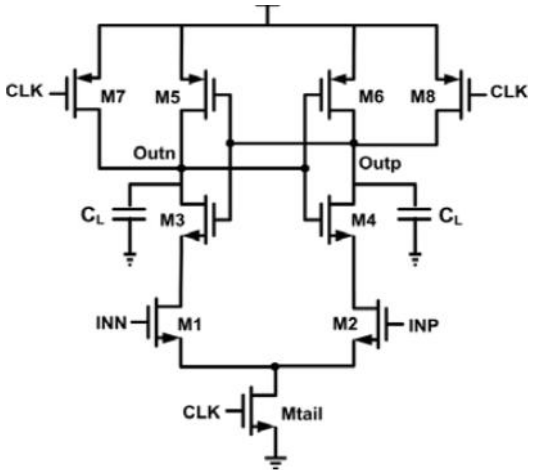

Fig. 2. Schematic diagram of the conventional dynamic comparator.

A. Conventional Dynamic Comparator

The schematic diagram of the conventional dynamic comparator widely used in A/D converters, with high input impedance, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [1], [17]. The operation of the comparator is as follows. During the reset phase when CLK = 0 and *M*tail is off, reset transistors (*M*7–*M*8) pull both output nodes Out*n* and Out*p* to *V*DD to define a start condition and to have a valid logical level during reset. In the comparison phase, when CLK = *V*DD, transistors *M*7 and *M*8 are off, and *M*tail is on. Output voltages (Out*p*, Out*n*), which had been pre-charged to *V*DD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP). Assuming the case where *V*INP > *V*INN, Out*p* discharges faster than Out*n*, hence when Out*p* (discharged by transistor *M*2 drain current), falls down to *V*DD |*V*thp| before Out*n* (discharged by transistor *M*1 drain current), the corresponding pMOS transistor (*M*5) will turn on initiating the latch regeneration caused by back-to-back inverters (*M*3, *M*5 and *M*4, *M*6). Thus, Out*n* pulls to *V*DD and Out*p* discharges to ground. If *V*INP < *V*INN, the circuits works vice versa. As shown in Fig. 2, the delay of this comparator is comprised of two time delays, *t*0 and *t*latch. The delay *t*0 represents the capacitive discharge of the load capacitance *C*L until the first p-channel transistor (*M*5/*M*6) turns on. In case, the voltage at node INP is bigger than INN (i.e., *V*INP > *V*INN), the drain current of transistor *M*2 (*I*2) causes faster discharge of Out*p* node compared to the Out*n* node, which is driven by *M*1 with smaller current. Consequently, the discharge delay (*t*0) is given by

$$t0 = \frac{CL|Vthp|}{I2} \qquad (1)$$

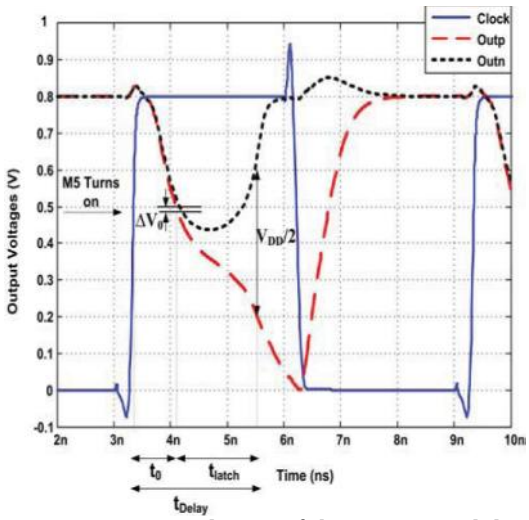

Fig.3.Transient simulations of the conventional dynamic comparator for input voltage difference of *V*in = 5 mV, *V*cm = 0.7 V, and *V*DD = 0.8 V.

In (1), since *I*2 = *I*tail/2 + _*I*in = *I*tail/2 + *g*m1,2 Δ*V*in, for small differential input (Δ*V*in), *I*2 can be approximated to be constant and equal to the half of the tail current. The second term, *t*latch, is the latching delay of two cross coupled inverters. It is assumed that a voltage swing of *V*out = *V*DD/2 has to be obtained from an initial output voltage difference *V*0 at the falling output (e.g., Out*p*). Half of the supply voltage is considered to be the threshold voltage of the comparator following inverter or SR latch [17]. Hence, the latch delay time is given by, [18]

$$t_{latch} = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) = \frac{C_L}{g_{m,eff}} \cdot \ln\left(\frac{V_{DD}/2}{\Delta V_0}\right)$$

where *gm*,eff is the effective trans conductance of the back-to back inverters. In fact, this delay depends, in alogarithmic manner, on the initial output voltage difference at the beginning of the regeneration (i.e., at *t* = *t*0). Based on (1), _*V*0 can be calculated from (3)

$$V0 = Voutp(t-t0) - Voutn(t-t0)$$
$$= |Vthp| - \frac{I2t0}{CL} \qquad (2)$$

The current difference, Δ*I*in = |*I*1 − *I*2|, between the branches is much smaller than *I*1 and *I*2. Thus, *I*1 can be approximated by *I*tail/2 and (3) can be rewritten as

$$V0 = |Vthp| \frac{Iin}{I1} \qquad (3)$$

In principle, this structure has the advantages of high input impedance, rail-to-rail output swing, no static power consumption, and good robustness against noise and mismatch [1]. Due to the fact that parasitic capacitances of input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is the fact that due to several stacked transistors, a sufficiently high supply voltage is needed for a proper delay time. The reason is that, at the beginning of the decision, only transistors *M*3 and *M*4 of the latch contribute to the positive feedback until the voltage level of one output node has dropped below a level small enough to turn on transistors *M*5 or *M*6 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate-source voltage for transistors *M*3 and *M*4, where the gatesource voltage of *M*5 and *M*6 is also small; thus, the delay time of the latch becomes large due to lower transconductances.

Another important drawback of this structure is that there is only one current path, via tail transistor *M*tail, which defines the current for both the differential amplifier and the latch (the cross-coupled inverters). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval and a better Gm/I ratio, a large tail current would be desirable to enable fast regeneration in the latch [10]. Besides, as far as *M*tail operates mostly in triode region, the tail current depends on input common-mode voltage, which is not favorable for regeneration.

B. Conventional Double-Tail Dynamic Comparator

A conventional double-tail comparator is shown in Fig. 3 [10]. This topology has less stacking and therefore can operate at lower supply voltages compared to the conventional dynamic comparator. The double tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset [10].

The operation of this comparator is as follows (see Fig. 4). During reset phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During decision-making phase (CLK = *V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1/*C*fn(p) and on top of this, an input-dependent differential voltage *V*fn(p) will build up. The intermediate stage formed by *M*R1 and *M*R2 passes Δ*V*fn(p) to the crosscoupled inverters and also provides a good shielding between input and output, resulting in reduced value of kickback noise [10].

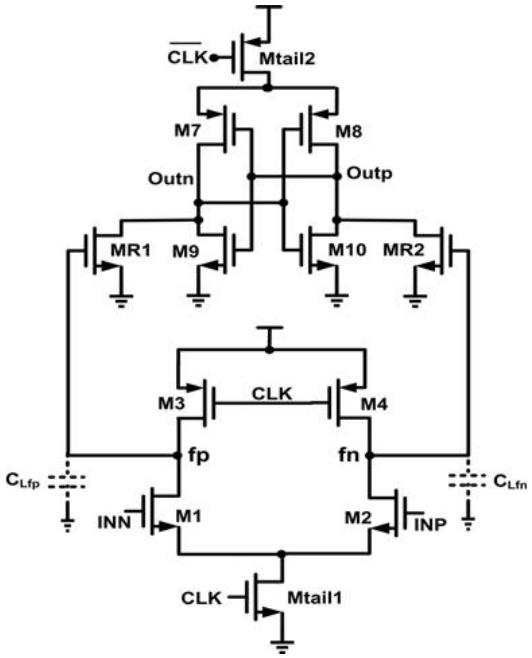

Fig.4. Schematic diagram of the conventional double-tail dynamic comparator.

Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, *t*0 and *t*latch. The delay *t*0 represents the capacitive charging of the load capacitance *CL*out (at the latch stage output nodes, Out*n* and Out*p*) until the first n-channel transistor (*M*9/*M*10) turns on, after which the latch regeneration starts; thus *t*0 is obtained from

$$t0 = \frac{V\text{Thn}CL\text{out}}{I\text{B1}} \approx 2\,\frac{V\text{Thn}CL\text{out}}{I\text{tail2}} \qquad (4)$$

where *I*B1 is the drain current of the *M*9 (assuming *V*INP > *V*INN, see Fig. 3) and is approximately equal to the half of the tail current (*I*tail2).

After the first n-channel transistor of the latch turns on (for instance, *M*9), the corresponding output (e.g., Out*n*) will be discharged to the ground, leading front p-channel transistor (e.g., *M*8) to turn on, charging another output (Out*p*) to the supply voltage (*V*DD). The regeneration time (*t*latch) is achieved according to (2).For initial output voltage difference at time t0, ΔV0 we have

$$\Delta V0 = V\text{thn}\,\frac{\Delta I\ \text{latch}}{I\text{B1}} = 2V\text{thn}\,\frac{g\text{mR1,2}}{I\text{tail2}}\,\Delta V0\text{fn/fp} \qquad (5)$$

where *g*mR1,2 is the trans conductance of the intermediate stage transistors (*M*R1 and *M*R2) and *V*fn/fp is

the voltage difference at the first stage outputs (fn and fp) at time *t*0. Thus, it can be concluded that two main parameters which influence the initial output differential voltage (Δ*V*0 and thereby the latch regeneration time are the transconductance of the intermediate stage transistors (*g*mR1,2) and the voltage difference at the first stage outputs (fn and fp) at time *t*0.

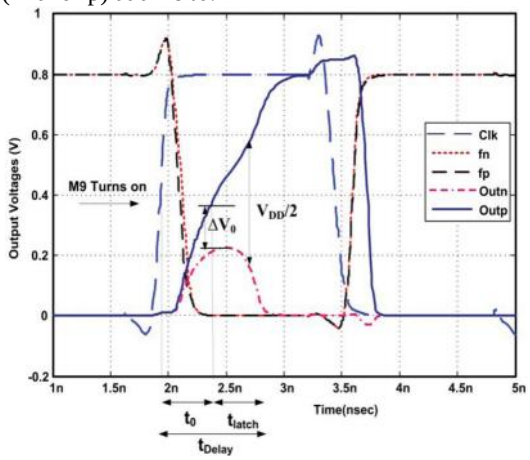

Fig. 5. Transient simulations of the conventional double-tail dynamic comparator for input voltage difference of Δ*V*in = 5mV, *V*cm = 0.7 V, and *V*DD = 0.8 V.

The differential voltage at nodes fn/fp (ΔVfn/fp) at time *t*0 can be achieved from

$$\Delta Vfn/fp = t0.\ \frac{IN1-IN2}{CL,fn(p)} \qquad (6)$$

In this equation, *I*N1 and *I*N2 refer to the discharging currents of input transistors (*M*1 and *M*2), which are dependent on the input differential voltage (i.e., Δ*I*N = *g*m1, Δ*V*in).Substituting (9) in (8), Δ*V*0 will be

$$\Delta V0 = 2Vthn\ \frac{gmR1,2}{Itail2}\ \Delta V0fn/fp \qquad (7)$$

This equation shows that Δ*V*0 depends strongly on the transconductance of input and intermediate stage transistors, input voltage difference (Δ*V*in), latch tail current, and the capacitive ratio of *CL*out to *CL*,fn(p). Substituting Δ*V*0 in latch regeneration time (2), the total delay of this comparator is achieved as follows:

tdelay=t0+tlatch

$$= 2\ \frac{VThn\ CLout}{Itail2} + \frac{CLout.}{gm,eff}\ ln(VDD/2) \qquad (8)$$

From the equations derived for the delay of the double-tail dynamic comparator, some important notes can be concluded.

1) The voltage difference at the first stage outputs (Δ*V*fn/fp) at time *t*0 has a profound effect on latch initial differential output voltage (Δ*V*0) and consequently on the latch delay. Therefore, increasing it would profoundly reduce the delay of the comparator.

2) In this comparator, both intermediate stage transistors will be finally cut-off, (since fn and fp nodes both discharge to the ground), hence they do not play any role in improving the effective transconductance of the latch. Besides, during reset phase, these nodes have to be charged from ground to *V*DD, which means power consumption. The following section describes how the proposed comparator improves the performance of the double-tail comparator from the above points of view.

III.DYNAMIC DUAL RAIL DOUBLE TAIL LATCH COMPARATOR

Circuit Diagram of Proposed Comparator is shown in Figure 5. This circuit mainly is a derived version of the [5]. The back-to-back latch stage is replaced with back-to-back dual input single output differential amplifier. Differential amplifier has so many advantages over the conventional latch which nothing but an inverter. It has higher immunity to
environmental noise and it rejects common mode noise or in other words it has better CMRR. Another property of differential signaling is the increase in maximum achievable voltage swings. It also provides simpler biasing and higher linearity. Main purpose is to eliminating the noise that is present in the latch stage and for which output is
getting fluctuated with clock transition.

OPERATION OF THE PROPOSED COMPARATOR

During reset phase (clk= 0V), PMOS transistor M4 and M5 turn on and they charge node voltages to VDD. And Hence NMOS transistors M17 and M19 turns on and discharges nodes voltages to GND. Then M14, M15 and PMOS transistors of differential amplifier blocks M12 and M13 turns on, NMOS transistors of differential amplifier block M8, M9 and M6, M7 turns off. The out nodes are charges to VDD.

During evaluation phase (clk= VDD), the node capacitances are discharged from VDD to GND in a rate which is proportional to the input voltages. At a certain voltage of Ni nodes, the inverter pairs M16 /M17 and M18/M19 invert the node signal

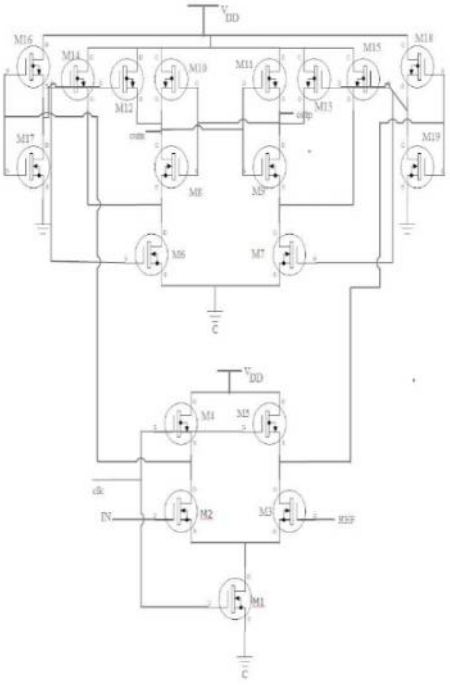

Fig. 6. Schematic diagram of the conventional dynamic dual rail double tail latch Comparator.

into a regenerated signal. These regenerated signals turn PMOS transistors M14, M12, M13, and M15 off. And eventually M6, M7, turns on. Hence the back-to-back differential pair again regenerates the node signals and because of M6 and M7 being on, the output latch stage converts the small voltage difference transmitted from node into a full scale digital level output.

IV. RESULT

In order to compare the proposed comparator with the conventional and double-tail dynamic comparators, all circuits have been simulated with *V*DD = 1V. The comparators were optimized and the transistor dimensions were scaled to get an equal offset standard variation of σOS = 8 mV at the input common mode voltage of *V* cm = 1.1 V (the same conditions that are found in [10]).

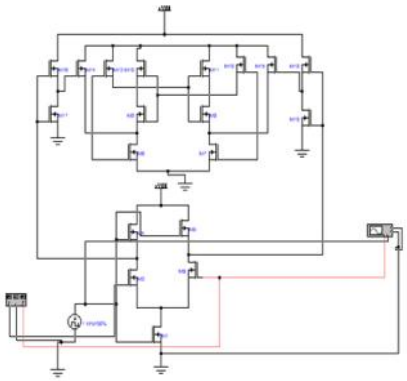

Fig.7. Dynamic dual rail double tail latch Comparator using PSPICE.

V.CONCLUSION

A new dynamic comparator using positive feedback shows higher speed, lower power dissipation than the conventional dynamic latched comparators has been proposed & targeted for ADC application. The results are simulated in PSPICE with 90nm CMOS technology. In the proposed design, the back-to-back inverter is replaced with dual input single output differential amplifier in the latched stage. Output of the latch stage in the proposed design is not affected by noise. The noise present in the input and the clock is completely suppressed by the differential amplifiers present in the output latch stage. The proposed structure shows significantly lower power dissipation, higher speed compared to the dynamic comparators present in the literature. The transistor count in the proposed comparator is higher to an extent among all the comparators analyzed.

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